PM7384

FREEDM™-84P672

FRAME ENGINE AND DATALINK MANAGER 84P672

PROGRAMMER'S GUIDE

PROPRIETARY AND CONFIDENTIAL

ADVANCE

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1 INTRODUCTION

1.1 Scope

The FREEDM-84P672 Programmer's Guide describes the configurable features and operation of a FREEDM-84P672 from a programmer's perspective. This document may not cover all applications of the FREEDM-84P672. Please contact a PMC-Sierra Applications Engineer for specific uses not covered in this document.

This document is a supplement to the FREEDM-84P672 Longform Datasheet[1]. Both documents should be studied together to interface the FREEDM-84P672 to an embedded processor. In case of a discrepancy between the Programmer's Guide and the Longform Datasheet, the Longform Datasheet shall always be considered correct.

1.2 Target Audience

The FREEDM-84P672 Programmer's Guide describes the data structures and initialisation necessary for programming the FREEDM-84P672 from a programmer's perspective. This document has been prepared for readers with prior knowledge of the HDLC protocol.

Although the examples provided in this document are described in C language syntax, they are not meant as compile-ready code segments.

1.3 Numbering Conventions

The following numbering conventions are used throughout this document:

binary	011 1010B, 011
decimal	129, 6, 12
hexadecimal	0x1FE2, 09FH

1.4 Register Description

Unless specified, FREEDM-84P672 registers are described using the convention **REGISTER_NAME** (byte offset from base address). There are two register spaces that can be addressed on a FREEDM-84P672 – they are the normal mode registers and the PCI configuration registers.

1.4.1 Normal Mode Registers

Normal mode registers are used to configure, monitor and control the operation of the FREEDM-84P672. Registers must be accessed as 32-bit values with a dword aligned address. A register value is accessed through the PCI Host interface during a PCI bus read, or write transaction, and has the following characteristics:

- Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits should be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software during a register read access.

- Except where noted, all configuration bits that can be written into can also be read back. This allows the processor controlling the FREEDM-84P672 to determine the programming state of the block.

- Writable normal mode registers are cleared to logic zero upon reset unless otherwise noted.

- Writing into read-only normal mode register bit locations does not affect FREEDM-84P672 operation unless otherwise noted.

- Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the FREEDM-84P672 operates as intended, reserved register bits must only be written with their default values. Similarly, writing to reserved registers should be avoided.

1.4.2 PCI Configuration Registers

PCI configuration registers are defined by the PCI SIG[2] and are used to install and configure devices on the PCI bus. Registers must be accessed as 32-bit values with a dword aligned address. A register value is only accessed through the PCI Host interface during a PCI configuration cycle, and has the following characteristics:

- Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

- Except where noted, all configuration bits that can be written into can also be read back. This allows the processor controlling the FREEDM-84P672 to determine the programming state of the block.

- Writable PCI configuration register bits are cleared to logic zero upon reset unless otherwise noted.

- Writing into read-only PCI configuration register bit locations does not affect FREEDM-84P672 operation unless otherwise noted.

- Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the FREEDM-84P672 operates as intended, reserved register bits must only be written with their default values. Similarly, writing to reserved registers should be avoided.

2 REFERENCES

1. PMC-990445, PMC-Sierra, Inc., "Frame Engine and Data Link Manager 84P672" Longform Datasheet, April 1999, Issue 1.

2. PCI Special Interest Group, PCI Local Bus Specification, June 1, 1995, Version 2.1.

3. PMC-960758, PMC-Sierra, Inc., "Frame Engine and Data Link Manager" Longform Datasheet, May 1998, Issue 5.

4. PMC-980577, PMC-Sierra, Inc., "Saturn Compatible Scaleable Bandwidth Interconnect (SBI) Specification", October 1998, Issue 3.

5. PMC-990262, PMC-Sierra, Inc., "Frame Engine and Data Link Manager 32P672" Longform Datasheet, May 1999, Issue 2.

3 FREEDM-84P672 OVERVIEW

3.1 FREEDM-84P672 Summary

The PM7384 FREEDM-84P672 Frame Engine and Datalink Manager is an advanced data link layer processor that is ideal for applications such as IETF PPP interfaces for routers, Frame Relay switches and multiplexors, ATM switches and multiplexors, Internet/Intranet access equipment, packet-based DSLAM equipment, Packet over SONET, and PPP over SONET. The FREEDM-84P672 implements HDLC processing and PCI Bus memory management functions for a maximum of 672 bi-directional channels. The functional blocks of the FREEDM-84P672 are illustrated in Figure 1.

The FREEDM-84P672 may be configured to support channelised T1/J1/E1 or unchannelised DS-3 traffic on up to 84 links conveyed via a Scaleable Bandwidth Interconnect (SBI) interface. The SBI interface transports data in three Synchronous Payload Envelopes (SPEs), each of which may be configured independently to carry either 28 T1/J1 links, 21 E1 links or a single DS-3 link.

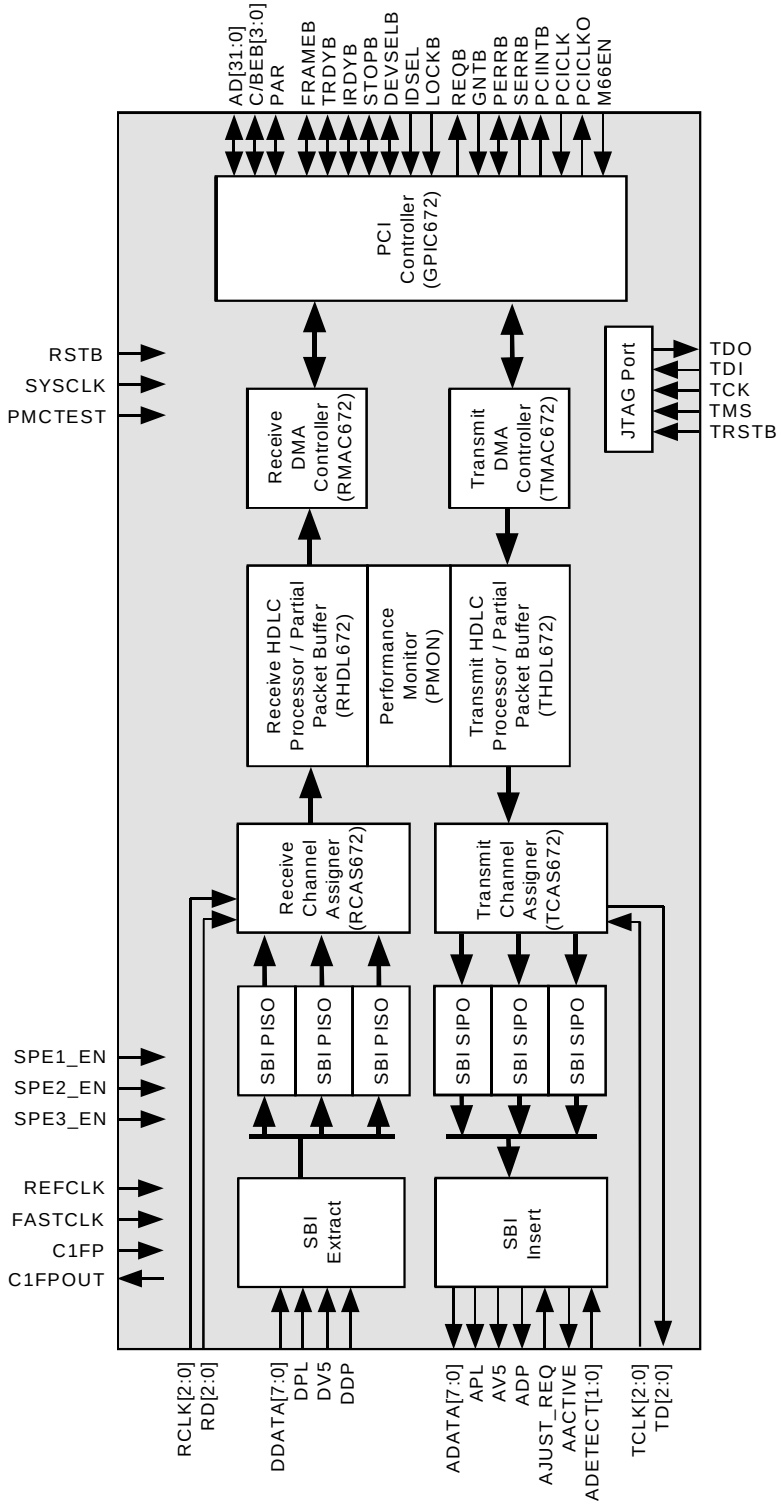
For channelised T1/J1/E1 links, the FREEDM-84P672 allows up to 672 bi-directional HDLC channels to be assigned to individual time-slots within each independently timed T1/J1 or E1 link. These links are processed by the Receive Channel Assigner (RCAS672) and the Transmit Channel Assigner (TCAS672). The channel assignment supports the concatenation of time-slots (N x DS0) up to a maximum of 24 concatenated time-slots for a T1/J1 link and 31 concatenated time-slots for an E1 link. Time-slots assigned to any particular channel need not be contiguous within a T1/J1 or E1 link. Unchannelised DS-3 links are assigned to a single HDLC channel.

Additionally, links may be configured independently to operate in an unframed or "clear channel" mode, in which the bit periods which are normally reserved for framing information in fact carry HDLC data. In unframed mode, links operate as unchannelised (i.e. the entire link is assigned to a single HDLC channel) regardless of link rate.

The FREEDM-84P672 supports mixing of channelised T1/J1/E1 and unchannelised or unframed links. The total number of channels in each direction is limited to 672. The maximum possible data rate over all links is 134.208 Mbps (which occurs with three DS-3 links running in unframed mode).

The FREEDM-84P672 supports three independently timed bidirectional clock/ data links, each carrying a single unchannelised HDLC stream. The links can be of arbitrary frame format and can operate at up to 52 MHz provided SYSCLK is

Figure 1 – FREEDM-84P672 Block Diagram



running at 40 MHz. When activated, each link replaces one of the SPEs conveyed on the SBI interface. (The maximum possible data rate when all three clock/data links are activated is 156 Mbps.)

Each data stream can be HDLC processed on a channelised basis within the Receive HDLC Processor / Partial Packet Buffer (RHDL672) and Transmit HDLC Processor / Partial Packet Buffer (THDL672). There is a 32 Kbyte buffer in the RHDL672 and another 32 Kbyte buffer in the THDL672 that must be assigned to FREEDM-84P672 channels to serve as channel FIFO's. Each buffer is a group of 2048 blocks with 16 bytes per block, and a minimum of 3 blocks must be assigned to a channel during provisioning. This allows for flexible assignment of a channel FIFO based on the expected data rate for the channel.

Alternatively, the RHDL672 and THDL672 can provision a channel as transparent, in which case, the raw data stream is transferred without HDLC processing.

The FREEDM-84P672 interfaces to an embedded processor and packet memory through the PCI local bus[2]. The packet memory provides buffer locations where the receive data is written to, and where the transmit data is read from. Data is organized into packets on a per channel basis within the packet memory. The Receive DMA Controller (RMAC672), the Transmit DMA Controller (TMAC672) and the General-Purpose PCI Controller (GPIC672) blocks perform the DMA of buffer data across the PCI local bus.

Each channel provisioned within the FREEDM-84P672 contends for access to the PCI bus based on its configuration within the RMAC672 and TMAC672 blocks. This provides the designer with the flexibility to individually configure each channel to avoid receive overrun or transmit underrun, based on the channel data rate.

The PMON block provides performance monitor counts for a number of events. These counters can be read via the PCI interface and provides a means for the host software to accumulate performance statistics.

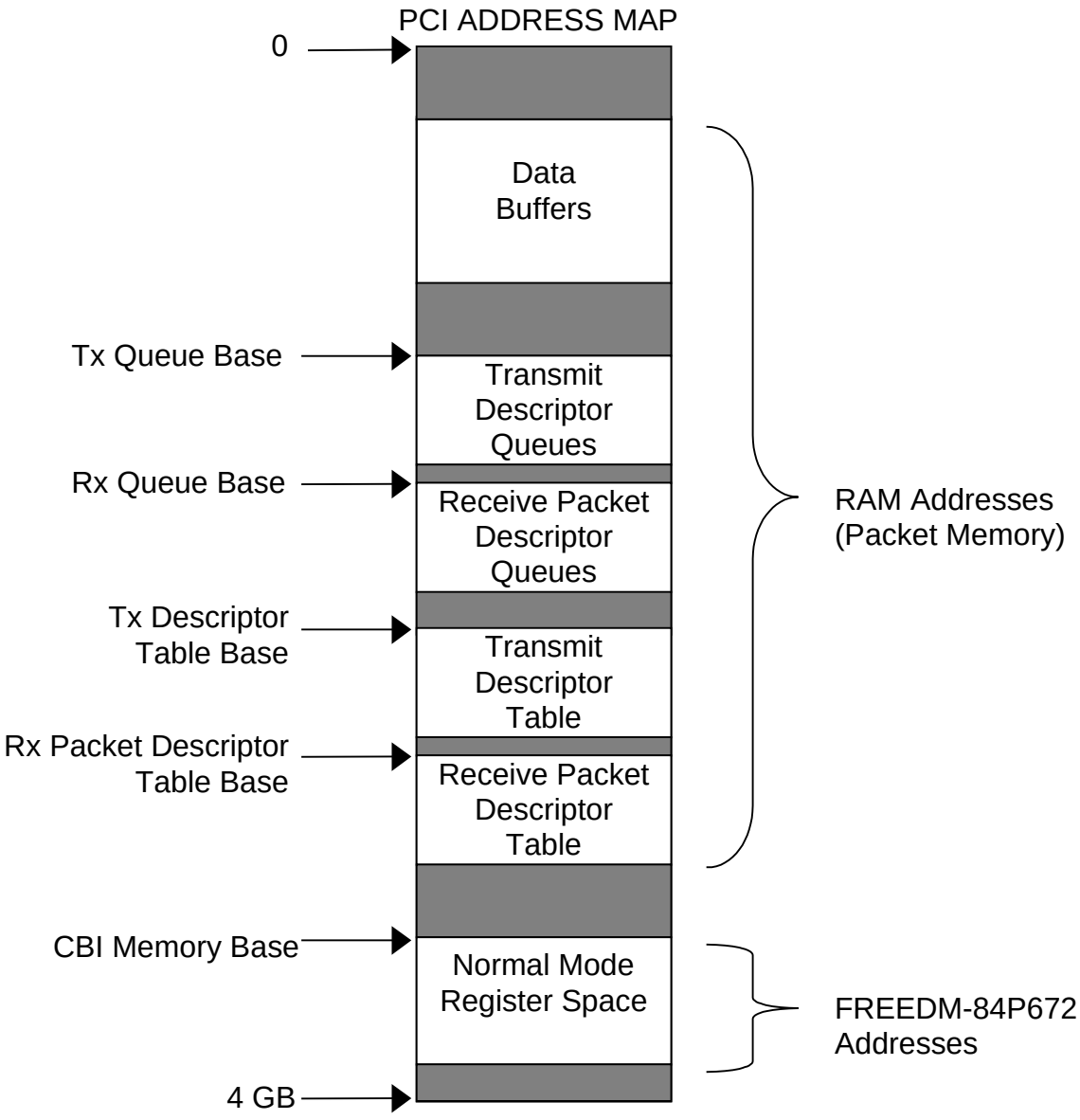
Links can be individually placed in line loopback. There is also an internal diagnostic loopback configuration for each channel which can be used to diagnose FREEDM-84P672 operation on a per channel basis.

3.2 PCI Interface

Figure 2 shows an address map for a PCI bus which contains one FREEDM-84P672 device. These data structures are required to interface a FREEDM-

84P672 to the PCI bus. In this figure, PCI addresses are 32-bit physical addresses which can be observed at the address pins of the bus.

Figure 2 – PCI Address Map



When multiple FREEDM-84P672's are attached to the bus, each FREEDM-84P672 must have a unique set of the following data structures:

- Transmit Descriptor Table

- Receive Packet Descriptor Table
- Transmit Queue Space
- Receive Queue Space
- Normal Mode Register Space

The data structures within RAM are accessed by software running on the embedded processor, or by the FREEDM-84P672. The software must specify the location of these data structures by writing base addresses into the appropriate FREEDM-84P672 registers before activating the FREEDM-84P672.

The FREEDM-84P672 accesses RAM directly using physical addressing whereas the software may use virtual addressing. In systems which use virtual memory management, the software must translate between virtual addresses (i.e. - pointers) and physical addresses. The software must ensure that the values written to FREEDM-84P672 registers are physical addresses rather than virtual addresses. In systems that do not use virtual addressing, or in systems where virtual addresses are identical to physical addresses, no address translation is required.

The Data Buffers are written with receive data by the FREEDM-84P672, or contain transmit data which is read by the FREEDM-84P672. The descriptor tables and the queues are required to manage these buffers.

The Normal Mode Register space is accessed by the software running on the embedded processor to manage and control operation of a FREEDM-84P672 device. This register space is located in the FREEDM-84P672 and is mapped into the PCI address space by the software.

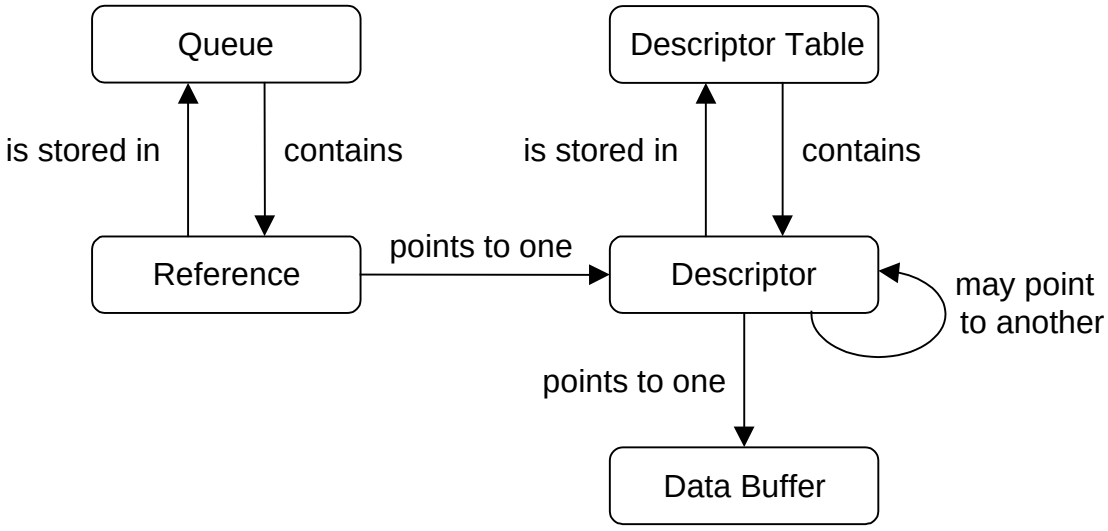
The PCI Configuration Space does not reside in the PCI address map, but it is a requirement for all PCI devices. The Configuration Space is a block of 256 contiguous bytes that reside in the PCI device, and is accessed by the embedded processor in a PCI bus Configuration Read (or Write) transaction, rather than a Memory Read (or Write) transaction. Access to this configuration space is system specific and a thorough discussion of it can be found in the PCI specification[2]. The PCI Configuration Space is discussed in section 6 of this document.

4 DATA STRUCTURES

The RAM data structures accessed by the FREEDM-84P672 are descriptors, descriptor tables, references and queues. The general relationship among them is shown in Figure 3.

In this figure, the direction of the arrows refers to the direction of the relationship. For example, each reference can point to one descriptor. Also, one descriptor may point to another descriptor, thereby specifying a linked-list of descriptors.

Figure 3 – Data Structure Relationships



These data structures are also accessed by software. The queues specify the data which may be accessed by the FREEDM-84P672 or the software, but not both simultaneously.

A Receive Packet consists of a reference pointing to one receive packet descriptor (RPD), or a linked-list of RPDs. A Transmit Packet consists of a reference pointing to one transmit descriptor (TD), or a linked-list of TDs. Transmit Packets may be linked by software, or by the FREEDM-84P672, via separate fields within each descriptor.

4.1 Descriptor Table

The descriptor table is essentially an array, whereby each element of the array is a descriptor and an index to the array is a reference.

A descriptor table holds descriptors of the same kind. The two descriptor tables are the Receive Packet Descriptor Table for receive packets, and the Transmit Descriptor Table for transmit packets.

Allocating a Descriptor Table

A descriptor table can be located anywhere within a 32-bit address space and must be aligned on a 16 byte boundary. The memory allocation must specify a fixed memory address space that cannot be swapped or moved by the operating system.

The size of a descriptor table is specified by the software during initialization. The number of references associated with a FREEDM-84P672 determines the size of the descriptor table. The relationship is: Size (in bytes) = 16* Number of References.

The table index (reference) is a 15-bit value which limits the size to 32,768 descriptors, or 524,288 bytes. The minimum size of the descriptor table depends on the number of channels provisioned. For a descriptor table where each packet is represented by one descriptor, the number of references must be at least 3 times the number of channels provisioned. If the number of descriptors used to represent a packet is greater than one, then the number of references must increase in proportion.

The following FREEDM-84P672 registers must be written with the physical address of the Receive Descriptor Table and the Transmit Descriptor Table, respectively:

Bit	Register
RPDTB[15:0]	**RMAC Packet Descriptor Table Base LSW** (0x288)
RPDTB[31:16]	**RMAC Packet Descriptor Table Base MSW** (0x28C)
TDTB[15:0]	**TMAC Transmit Descriptor Table Base LSW** (0x308)
TDTB[31:16]	**TMAC Transmit Descriptor Table Base MSW** (0x30C)

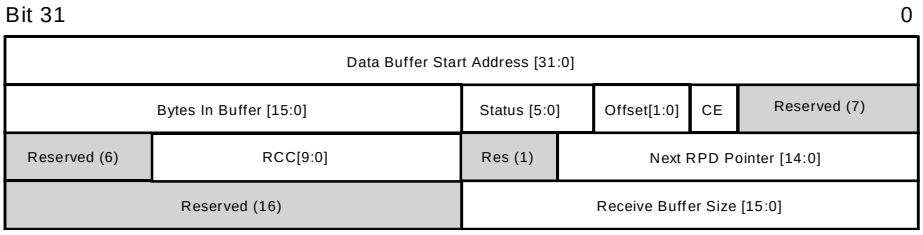
Note: RPDTB[3:0] and TDTB[3:0] must be zero, in order to align the descriptor tables on 16 byte boundaries.

4.2 Receive Packet Descriptor

A Receive Packet Descriptor (RPD) is a 16 byte data structure that contains a number of fields as shown in Figure 4. RPDs are used in the receive direction to describe packets that are received and written to packet memory. Each RPD is

located in the Receive Packet Descriptor Table and is indexed from the base address using a RPD Reference (RPDR).

Figure 4 – Receive Packet Descriptor



The following table describes the individual fields within each RPD:

Field	Description
Data Buffer Start Address[31:0]	The Data Buffer Start Address[31:0] bits point to the data buffer in host memory. This field is expected to be configured by the Host during initialisation. The Data Buffer Start Address field is valid in all RPDs.
CE	The Chain End (CE) bit indicates the end of a linked list of RPDs. When CE is set to logic one, the current RPD is the last RPD of a linked list of RPDs. When CE is set to logic zero, the current RPD is not the last RPD of a linked list. The CE bit is valid for all RPDs written by the RMAC672 to the Receive Ready Queue. When a packet requires only one RPD, the CE bit is set to logic one. The CE bit is ignored for all RPDs read by the RMAC672 from the Receive Free Queues, each of which is assumed to point to only one buffer, i.e. not a chain.
Offset[1:0]	The Offset[1:0] bits indicate the byte offset of the data packet from the start of the buffer. If this value is non-zero, there will be 'dummy' (i.e. undefined) bytes at the start of the data buffer prior to the packet data proper. For a linked list of RPDs, only the first RPD's Offset field is valid. All other RPD Offset fields of the linked list are set to 0.

Field	Description
Status [5:0]	The Status[5:0] bits indicate the status of the received packet. Status[0] Rx buffer overrun Status[1] Packet exceeds max. allowed size Status[2] CRC error Status[3] Packet Length not an exact no. of bytes Status[4] HDLC abort detected Status[5] Unused (set to 0) For a linked list of RPDs, only the last RPD's Status field is valid. All other RPD Status fields of the linked list are invalid and should be ignored. When a packet requires only one RPD, the Status field is valid.
Bytes in Buffer [15:0]	The Bytes in Buffer[15:0] bits indicate the number of bytes actually used in the current RPD's data buffer to store packet data. The count excludes the 'dummy' bytes inserted as a result of a non-zero Offset field. A count greater than 32767 bytes indicates a packet that is shorter than the expected length of the FCS field. The Bytes in Buffer field is invalid when Status[0] or Status[4] is asserted .
Next RPD Pointer [14:0]	The Next RPD Pointer[14:0] bits store a RPDR which enables the RMAC672 to support linked lists of RPDs. This field, which is only valid when CE is equal to logic zero, contains the RPDR to the next RPD in a linked list. The RMAC672 links RPDs when more than one buffer is needed to store a packet. The Next RPD Pointer is not valid for the last RPD in a linked list (when CE=1). When a packet requires only one RPD, the Next RPD Pointer field is not valid.
RCC[9:0]	The Receive Channel Code (RCC[9:0]) bits are used by the RMAC672 to associate a RPD with a channel. For a linked list of RPDs, all the RPDs' RCC[9:0] fields are valid. i.e. all contain the same channel value.

Field	Description
Receive Buffer Size [15:0]	The Receive Buffer Size[15:0] bits indicate the size in bytes of the current RPD's data buffer. This field is expected to be configured by the Host during initialisation. The Receive Buffer Size must be a non-zero integer multiple of sixteen and less than or equal to 32752. The Receive Buffer Size field is valid in all RPDs.

Notes:

- For error checking purposes, it is recommended to examine the Bytes in Buffer[15:0] field to ensure that it does not exceed the Receive Buffer Size[15:0].
- The RPD for the FREEDM-84P672 is the same as for the FREEDM-32P672. Please see Appendix A for the differences in the RPD between the FREEDM-84P672 and the FREEDM-32.

Receive Packet Descriptor Fields Initialized By Software

The following fields of each RPD must be assigned before writing its reference to the RPDRF Large queue, or to the RPDRF Small queue:

Field	Value
Data Buffer Start Address	value is determined during run time or preconfigured
Receive Buffer Size	value is determined during run time or preconfigured

Receive Packet Descriptor Fields Modified By FREEDM-84P672

The following fields are modified by the FREEDM-84P672 after it reads the reference from the RPDRF Large queue, or from the RPDRF Small queue, but before the same reference is written to the RPDR Ready queue:

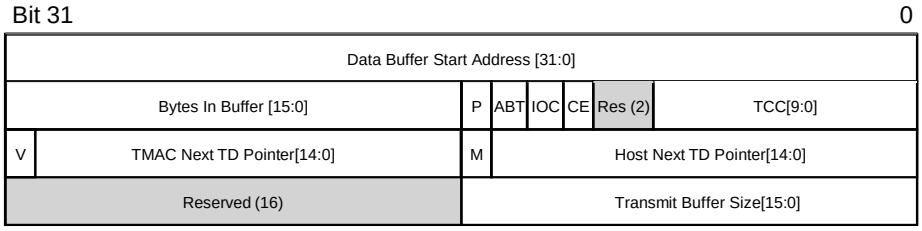
Field	Value
CE	value is determined during run time
Offset	value is determined during run time
Status	value is determined during run time
Bytes in Buffer	value is determined during run time

Field	Value
Next RPD Pointer	value is determined during run time
RCC	value is determined during run time

4.3 Transmit Descriptor

A Transmit Descriptor (TD) is a 16 byte data structure that contains a number of fields as shown in Figure 5. TDs are used in the transmit direction to describe packets that are read from packet memory and transmitted by the FREEDM-84P672. Each TD is located in the Transmit Descriptor Table and is indexed from the base address using a TD Reference (TDR).

Figure 5 – Transmit Descriptor



The following table describes the individual fields within each TD:

Field	Description
Data Buffer Start Address [31:0]	The Data Buffer Start Address[31:0] bits point to the data buffer in host memory. The Data Buffer Start Address field is valid in all TDs.
Bytes In Buffer [15:0]	The Bytes In Buffer[15:0] field is used by the host to indicate the total number of bytes to be transmitted in the current TD. Zero length buffers are illegal.

Field	Description
P	The Priority bit is set by the host to indicate the priority of the associated packet in a two level quality of service scheme. Packets with its P bit set high are queued in the high priority queue in the TMAC672. Packets with the P bit set low are queued in the low priority queue. Packets in the low priority queue will not begin transmission until the high priority queue is empty.
ABT	The Abort (ABT) bit is used by the host to abort the transmission of a packet. When ABT is set to logic 1, the packet will be aborted after all the data in the buffer has been transmitted. If ABT is set to logic 1 in the current TD, the M bit must be set low and the CE bit must be set to high.
IOC	The Interrupt On Complete (IOC) bit is used by the host to instruct the TMAC672 to interrupt the host when the current TD's data buffer has been read. When IOC is logic 1, the TMAC672 asserts the IOCI interrupt when the data buffer has been read. Additionally, the Free Queue FIFO will be flushed. If IOC is logic zero, the TMAC672 will not generate an interrupt and the Free Queue FIFO will operate normally.

Field	Description
CE	The Chain End (CE) bit is used by the host to indicate the end of a linked list of TDs presented to the TMAC672. The linked list can contain one or more packets as delineated by the M bit (see below). When CE is set to logic 1, the current TD is the last TD of a linked list of TDs. When CE is set to logic 0, the current TD is not the last TD of a linked list. When the current TD is not the last of the linked list, the Host Next TD Pointer[14:0] field is valid, otherwise the field is not valid. Note: When CE is set to logic 1, the only valid value for M is logic 0. Note: When presenting raw (i.e. unpacketised) data for transmission, the host should code the M and CE bits as for a single packet chain, i.e. M=1, CE=0 for all TDs except the last in the chain and M=0, CE=1 for the last TD in the chain.
TCC[9:0]	The Transmit Channel Code (TCC[9:0]) bits are used by the host to associate a channel with a TD pointed to by a TDR. All TCC[9:0] fields in a linked list of TDs must be set to the same value.
V	The V bit is used to indicate that the TMAC Next TD Pointer field is valid. When set to logic 1, the TMAC Next TD Pointer[14:0] field is valid. When V is set to logic 0, the TMAC Next TD Pointer[14:0] field is invalid. The V bit is used by the host to reclaim data buffers in the event that data presented to the TMAC672 is returned to the host due to a channel becoming unprovisioned. The V bit is expected to be initialised to logic 0 by the host.

Field	Description
TMAC Next TD Pointer [14:0]	The TMAC Next TD Pointer[14:0] bits are used to store TDRs which permits the TMAC672 to create linked lists of TDs passed to it via the TDRR queue. The TDs are linked with other TDs belonging to the same channel and same priority level. In the case that data presented to the TMAC672 is returned to the host due to a channel becoming unprovisioned, a TDR pointing to the start of the per-channel linked list of TDs is placed on the TDRF queue. It is the responsibility of the host to follow the TMAC672 and host links in order to recover all the buffers.
M	The More (M) bit is used by the host to support packets that require multiple TDs. If M is set to logic 1, the current TD is just one of several TDs for the current packet. If M is set to logic 0, this TD either describes the entire packet (in the single TD packet case) or describes the end of a packet (in the multiple TD packet case). Note: When M is set to logic 1, the only valid value for CE is logic 0.
Host Next TD Pointer [14:0]	The Host Next TD Pointer[14:0] bits are used to store TDRs which permits the host to support linked lists of TDs. As described above, linked lists of TDs are terminated by setting the CE bit to logic 1. Linked lists of TDs are used by the host to pass multiple TD packets or multiple packets associated with the same channel and priority level to the TMAC672.
Transmit Buffer Size [15:0]	The Transmit Buffer Size[15:0] field is used to indicate the size in bytes of the current TD's data buffer. (N.B. The TMAC672 does not make use of this field.)

Note: The TD for the FREEDM-84P672 is the same as for the FREEDM-32P672. Please see Appendix B for the differences in the TD between the FREEDM-84P672 and the FREEDM-32.

Transmit Descriptor Fields Initialized By Software

The following fields of a TD (or a linked-list of TDs) must be assigned before writing its reference to the TDR Ready queue:

Field	Value
Data Buffer Start Address	value is determined during run time or preconfigured
Bytes In Buffer	value is determined during run time or preconfigured
P	value is determined during run time or preconfigured
ABT	value is determined during run time or preconfigured
IOC	value is determined during run time or preconfigured
CE	value is determined during run time or preconfigured
TCC	value is determined during run time or preconfigured
V	0
M	value is determined during run time or preconfigured
Host Next TD Pointer	value is determined during run time or preconfigured

Transmit Descriptor Fields Modified By FREEDM-84P672

The following fields may be modified by the FREEDM-84P672 after it reads the reference from the TDR Ready queue, but before the same reference is written to the TDR Free queue:

Field	Value
V	value is determined during run time
TMAC Next TD Pointer	value is determined during run time

4.4 Data Buffers

In the receive path, the FREEDM-84P672 writes receive packet data into data buffers. In the transmit path, the FREEDM-84P672 reads transmit packet data

from data buffers. A buffer must be allocated and assigned to each descriptor by the software.

Allocation of Data Buffers

Buffers must be allocated in fixed memory. The receive data buffer size must be a non-zero integer multiple of 16 bytes, with a maximum size of 32,752 bytes and a minimum size of 16 bytes. There is no restriction for the address alignment of the buffers.

For a receive buffer, the following fields of a RPD must be assigned:

Field	Value
Data Buffer Start Address	value is determined during run time or preconfigured
Receive Buffer Size	value is determined during run time or preconfigured

For a transmit buffer, the following fields of a TD must be assigned:

Field	Value
Data Buffer Start Address	value is determined during run time or preconfigured
Bytes In Buffer	value is determined during run time or preconfigured

The FREEDM-84P672 automatically links RPDs when the receive packet length exceeds the buffer size.

The software must link TDs when the packet data is "scattered" among a number of buffers.

4.5 References

References are dword structures used to access descriptors within a descriptor table. They also have status bits which are written by the FREEDM-84P672 after it has processed the packet. The reference, including status bits, is written into a queue by the FREEDM-84P672 during a queue write operation. The status bits indicate the success of receive or transmit processing and should be checked by software when the reference is read from the queue.

4.5.1 Receive Packet Descriptor Reference

Each Receive Packet Descriptor Reference (RPDR) Ready Queue element is 32 bits in size, but only the least significant 17 bits are valid. The 17 least significant bits consist of a 15-bit RPDR and 2 status bits for the RPD pointed at by this RPDR. A RPDR has the following fields:

Bit 31 17	16 15	14 0
UNUSED	STATUS[1:0]	RPDR[14:0]

Field	Description
STATUS[1:0]	The encoding for the status field is as follows: 00 – Successful reception of packet. 01 – Unsuccessful reception of packet. 10 – Unprovisioned partial packet. 11 – Partial packet returned due to RAWMAX limit being reached.
RPDR[14:0]	The RPDR[14:0] field defines the offset of the first RPD in a linked chain of RPDs, each pointing to a buffer containing the received data.

When the RMAC672 writes a STATUS+RPDR to the RPDR Ready queue, it sets bits [23:17] of the queue element to all 0's and leaves bits [31:24] unmodified as follows:

Bit 31 24	23 17	16 15	14 0
UNMODIFIED	000 0000B	STATUS[1:0]	RPDR[14:0]

This may be useful to software which polls host memory to determine when a reference has been written into a queue, instead of responding to an interrupt and reading a FREEDM-84P672 register. The software should write a non-zero value to bits [23:17] after reading the reference, and at a later time it can check whether the non-zero value was overwritten by the FREEDM-84P672, indicating that the FREEDM-84P672 has written another reference into this queue location.

Note: Only one RPDR is written into the RPDR Ready queue per receive packet, and this RPDR represents the linked list of RPDs which identify the receive packet.

4.5.2 Transmit Descriptor Reference

Each Transmit Descriptor Reference (TDR) Free Queue element is 32 bits in size, but only the least significant 18 bits are valid. The 18 least significant bits consist of a 15-bit TDR and 3 status bits for the TD pointed at by this TDR. A TDR has the following fields:

Bit 31 18	17 15	14 0
UNUSED	STATUS[2:0]	TDR[14:0]

Field	Description
Status[2:0]	The TMAC672 fills in the Status field to indicate to the host the results of processing the TD. The encoding is: Status[1:0] Description 00 Last or only buffer of packet, buffer read. 01 Buffer of partial packet, buffer read. 10 Unprovisioned channel, buffer not read. 11 Malformed packet (e.g. Bytes In Buffer field set to 0), buffer not read. Status[2] Description 0 No underflow detected. 1 Underflow detected.
TDR[14:0]	The TDR[14:0] field contains the offset of the TD returned.

When the TMAC672 writes a STATUS+TDR into the TDR Free queue, it sets bits [23:18] of the queue element to all 0's and leaves bits [31:24] unmodified as follows:

Bit 31 24	23 18	17 15	14 0
UNMODIFIED	00 0000B	STATUS[2:0]	TDR[14:0]

This may be useful to software which polls host memory to determine when a reference has been written into a queue, instead of responding to an interrupt and reading a FREEDM-84P672 register. The software should write a non-zero value to bits [23:18] after reading the reference, and at a later time it can check whether the non-zero value was overwritten by the FREEDM-84P672, indicating that the FREEDM-84P672 has written another reference into this queue location.

Notes:

- The TDR associated with each TD of a transmit packet is written to the TDR Free queue. In the case of a packet with multiple TDs there will be multiple TDRs written to the TDR Free queue.
- The Status[2] field of a TDR can be used to identify the occurrence of an underflow condition on the channel associated with the TDR. The underflow may or may not have occurred on the buffer associated with the TDR read from the TDR Free queue.

4.5.3 Access to Descriptors

TDs or RPDs can be accessed using the index field of the reference and the base address of the descriptor table as illustrated by the pseudo code below:

```
/* Need to mask out the upper 17 bits of the descriptor reference to
 * extract the index field. */
#define      RPD_INDEX_MASK    0x00007FFF
#define      TD_INDEX_MASK     RPD_INDEX_MASK
#define      MUL_16_BYTES      4

index = RxReference & RPD_INDEX_MASK;

/* The address of the descriptor in the descriptor table
 * can be determined as shown below */
desc_addr =  desc_table_base_addr + (index << MUL_16_BYTES);
```

4.6 Queues

A queue is a FIFO buffer located in fixed memory that holds a number of references. The FREEDM-84P672 has 5 queues which must be allocated. There are 2 queues for TDRs and 3 queues for RPDRs. The software must allocate memory for each of these queues.

In the receive direction, there is the Receive Packet Descriptor Reference Free Small queue (RPDR Free Small queue), the Receive Packet Descriptor Reference Free Large queue (RPDR Free Large queue), and the Receive Packet Descriptor Reference Ready queue (RPDR Ready queue). The FREEDM-84P672 reads from the RPDR Free Small queue and the RPDR Free Large queue to get free buffers into which the receive data is written. When the receive operation is complete, the FREEDM-84P672 writes a RPDR to the RPDR Ready queue. The software reads from the RPDR Ready queue to process a receive packet, and it writes to the RPDR Free Small (or Large) queue to reuse the RPD for another packet.

The FREEDM-84P672 obtains free buffers from the RPDR Free Small (or Large) queue based on the following 2-step algorithm:

1. The first buffer into which the receive packet is written is obtained from the RPDR Free Small queue, and if this queue is empty it is obtained from the RPDR Free Large queue.

2. If the receive packet length exceeds the small buffer size then the additional receive data is written into buffers obtained from the RPDR Free Large queue. If the RPDR Free Large queue is empty then the additional buffers are obtained from the RPDR Free Small queue.

In the transmit direction, there is the Transmit Descriptor Reference Ready queue (TDR Ready queue) and the Transmit Descriptor Reference Free queue (TDR Free queue). The software writes a TDR to the TDR Ready queue when it wants the FREEDM-84P672 to transmit a packet. The FREEDM-84P672 reads from the TDR ready queue and starts to transmit the packet, and when it has completed the transmit operation, it writes the TDR to the TDR Free queue. The software reads from the TDR Free queue to confirm that the packet has been transmitted, and to reuse the TD for another packet.

The entity (either the software or the FREEDM-84P672) which reads from a queue and the entity which writes to a queue is as follows:

Queue	**Read By**	**Written By**
RPDR Free Large	FREEDM-84P672	Software
RPDR Free Small	FREEDM-84P672	Software
RPDR Ready	Software	FREEDM-84P672
TDR Free	Software	FREEDM-84P672
TDR Ready	FREEDM-84P672	Software

There are four indexes for each queue that are used to manage its state. These indexes are located in the FREEDM-84P672 Normal Mode Register space. The values are described as follows:

Index	Description
start	The start index marks the lowest address of the queue. This is the first location in the queue. This value should not be modified after initialization.
write	The write index is modified by the entity which writes to the queue. The write index marks the address where a reference can be written. After the reference is written this value is incremented.
read	The read index is modified by the entity which reads from the queue. The read index marks the last location accessed by the reading entity. After the reference is read this value is incremented.
end	The end index marks the address which follows the last location (the highest addressable location) in the queue. This value should not be modified after initialization.

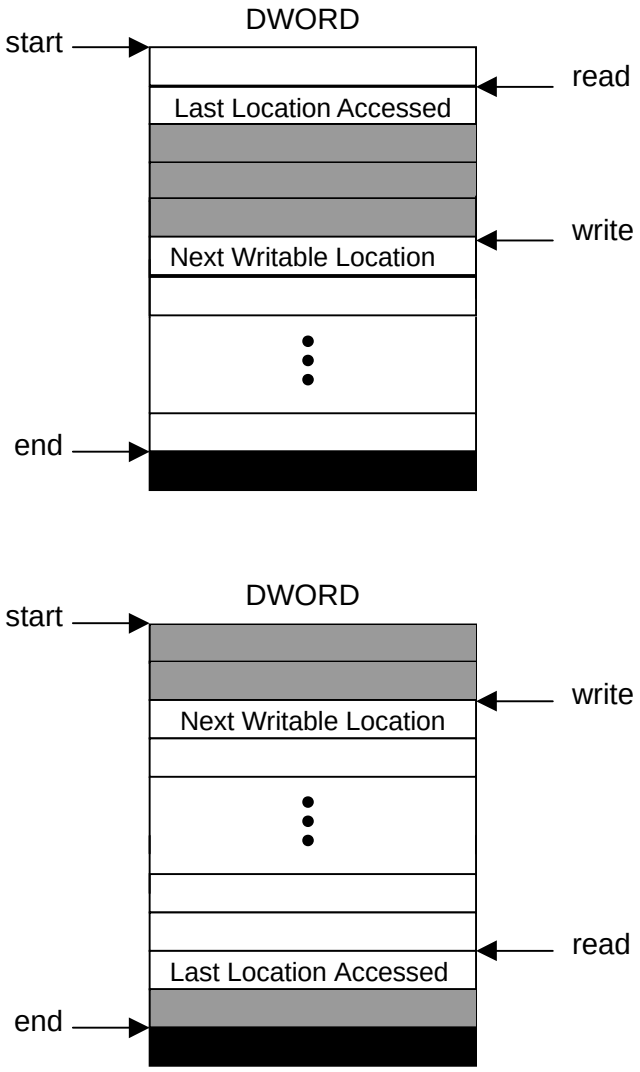
Note: The end index points to a location that is beyond the queue; a reference can not be read from or written to this location. However, the start index of one queue can be set to the end index of another queue.

The various queue entities (references) in Figures 6 to 8 are illustrated using the following legend:

	Empty Reference Location
	Valid Reference Location
	Invalid Reference Location for this Queue

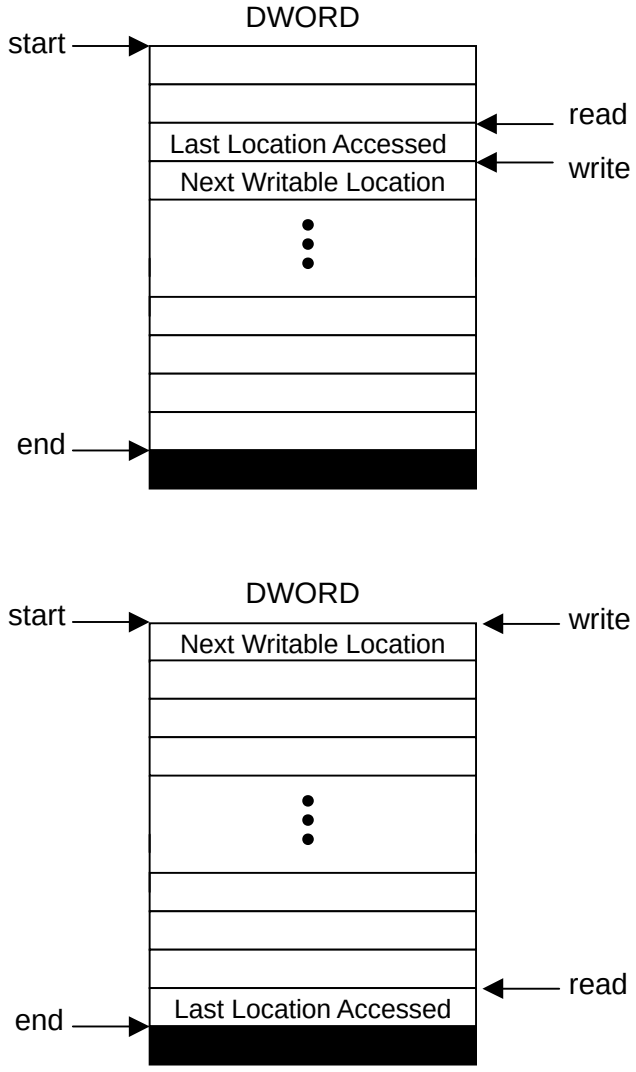
Some normal queue states are illustrated in Figure 6. Note the circular nature of the queues.

Figure 6 – Normal Queue States



The empty queue states are illustrated in Figure 7. The queue is empty when the read index is one location before the write index, or when the read index is one location before the end index and the write index equals the start index.

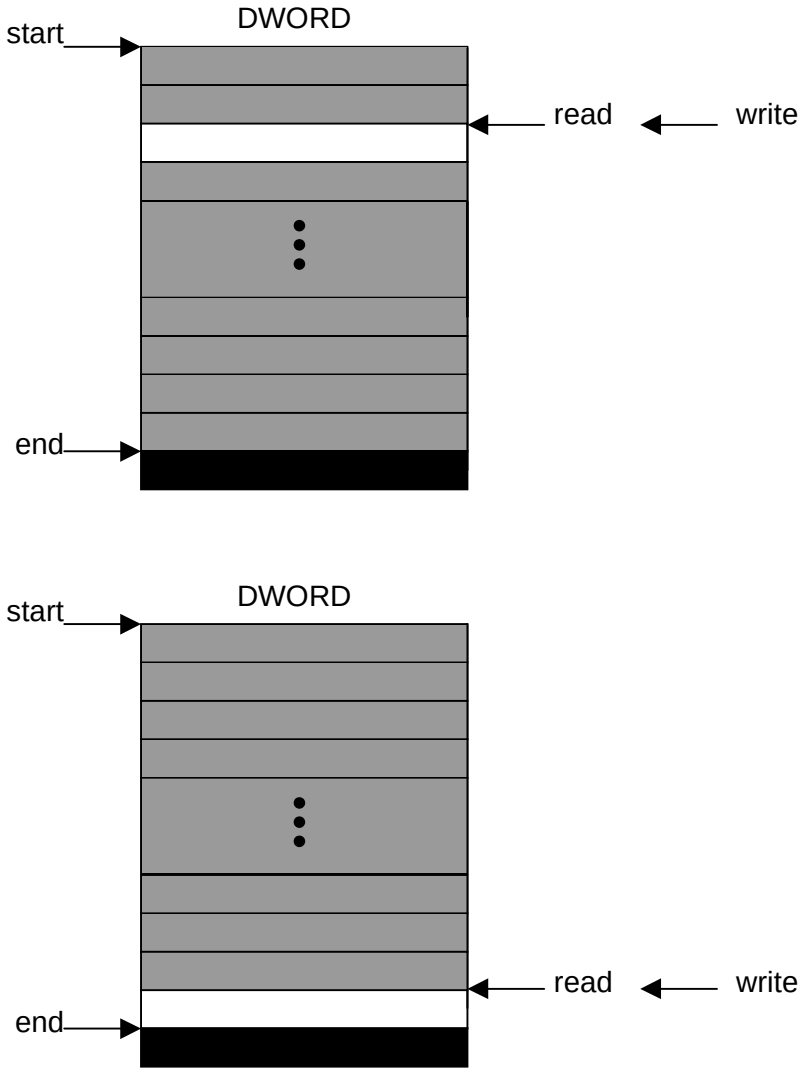
Figure 7 – Empty Queue States



The full queue states are illustrated in Figure 8. The queue is full when the read index is equal to the write index.

Figure 8 – Full Queue States

Allocation of Queues



From Figure 8, it can be seen that the physical size of a queue is one dword larger than the number of references in the queue when it is full. Therefore in order to create a queue that holds 128 references, the software must allocate contiguous memory of 129 dwords.

To obtain the best possible bus utilization, the size of a queue should not be too small, as this would lead to more frequent accesses to the read and/or write index registers of the FREEDM-84P672. The minimum recommended queue

size is approximately 32 references. In general, the queue should be large enough to hold one reference per provisioned channel.

The queues used for receive packets are located in fixed memory as offsets from a base address. The queues used for transmit packets are located in fixed memory as offsets from another base address. Base addresses must be dword aligned and are programmed as follows for the receive direction and transmit direction, respectively:

Bits	Register
RQB[15:0]	**RMAC Receive Queue Base LSW** (0x290)
RQB[31:16]	**RMAC Receive Queue Base MSW** (0x294)
TQB[15:0]	**TMAC Transmit Queue Base LSW** (0x310)
TQB[31:16]	**TMAC Transmit Queue Base MSW** (0x314)

The RPDR Free Large queue, the RPDR Free Small queue and the RPDR Ready queue must reside within 256Kbytes of the RMAC672 Receive Queue Base address. The size of each queue is specified by assignment of the start, write, read and end indexes.

The TDR Ready queue and the TDR Free queue must reside within 256Kbytes of the TMAC672 Transmit Queue Base address. The size of each queue is specified by assignment of the start, write, read and end indexes.

Initialization of Queues

The software must initialize each queue after the allocation procedure. Normally, a queue is initialized with the state shown below:

Queue	Initial State
RPDR Free Large	Full
RPDR Free Small	Full
RPDR Ready	Empty
TDR Free	Empty
TDR Ready	Empty

The software must write valid RPD References into the RPDRF Small (and Large) queues. The software may force the RMAC672 to store received data in buffers of only one size by setting one of the receive free queues to zero length

(i.e. – by setting the start and end index registers of one of the queues to equal values).

The software must also write the following FREEDM-84P672 registers with valid indexes:

Bits	Register
RPDRLFQS[15:0]	**RMAC Packet Descriptor Reference Large Buffer Free Queue Start** (0x298)
RPDRLFQW[15:0]	**RMAC Packet Descriptor Reference Large Buffer Free Queue Write** (0x29C)
RPDRLFQR[15:0]	**RMAC Packet Descriptor Reference Large Buffer Free Queue Read** (0x2A0)
RPDRLFQE[15:0]	**RMAC Packet Descriptor Reference Large Buffer Free Queue End** (0x2A4)
RPDRSFQS[15:0]	**RMAC Packet Descriptor Reference Small Buffer Free Queue Start** (0x2A8)
RPDRSFQW[15:0]	**RMAC Packet Descriptor Reference Small Buffer Free Queue Write** (0x2AC)
RPDRSFQR[15:0]	**RMAC Packet Descriptor Reference Small Buffer Free Queue Read** (0x2B0)
RPDRSFQE[15:0]	**RMAC Packet Descriptor Reference Small Buffer Free Queue End** (0x2B4)
RPDRRQS[15:0]	**RMAC Packet Descriptor Reference Ready Queue Start** (0x2B8)
RPDRRQW[15:0]	**RMAC Packet Descriptor Reference Ready Queue Write** (0x2BC)
RPDRRQR15:0]	**RMAC Packet Descriptor Reference Ready Queue Read** (0x2C0)
RPDRRQE[15:0]	**RMAC Packet Descriptor Reference Ready Queue End** (0x2C4)
TDRFQS[15:0]	**TMAC Transmit Descriptor Reference Free Queue Start** (0x318)
TDRFQW[15:0]	**TMAC Transmit Descriptor Reference Free Queue Write** (0x31C)
TDRFQR[15:0]	**TMAC Transmit Descriptor Reference Free Queue Read** (0x320)

Bits	Register
TDRFQE[15:0]	**TMAC Transmit Descriptor Reference Free Queue End** (0x324)
TDRRQS[15:0]	**TMAC Transmit Descriptor Reference Ready Queue Start** (0x328)
TDRRQW[15:0]	**TMAC Transmit Descriptor Reference Ready Queue Write** (0x32C)
TDRRQR[15:0]	**TMAC Transmit Descriptor Reference Ready Queue Read** (0x330)
TDRRQE[15:0]	**TMAC Transmit Descriptor Reference Ready Queue End** (0x334)

Queue Operation

The following code illustrates how the software can access a queue. It should be noted for a specific queue that the software will only read from it or write to it, but not both read and write to it.

```
#define QUEUE_BATCH_SIZE                          6

#define READ_INDEX_REGISTER(address)              ((*address)&0xFFFF)
#define WRITE_INDEX_REGISTER(address,value)       *address = (dword) value

BOOL ReadQueue(dword* pReference)
{
    dword* pQueueElement;

    /* The following code segment ensures the write index register
     * is not read too frequently. Thereby, minimizing
     * utilization of the PCI bus. */

    if (Headroom == 0) {
       /* Headroom was initialized to zero, and must be reinitialized
        * to a non-zero value in the following code segment before
        * the software is able to read a reference from the queue.
        * The Headroom is the number of references in the queue when the
        * write index was last read by software, minus the number of
        * these references that have been read. */
       Write = READ_INDEX_REGISTER(pWriteRegister);
       if (Write <= Read)
             Headroom = Write - Start + End - Read - 1;
       else
             Headroom = Write - Read - 1;
```

```
            /* Exit if the queue is empty */
            if (Headroom == 0) return FALSE;
        }
        Headroom--;

        /* Determine the read index of the reference in the queue.
         * Reading is a pre-increment operation. */
        Read++;
        if (Read == End)
            Read = Start;

        /* Read the reference from a RAM location */
        pQueueElement = pQueueBaseAddress + Read;
        *pReference = *pQueueElement;

        /* The following code segment ensures the read index register
         * is not written too frequently. Thereby, minimizing
         * utilization of the PCI bus. */

        if (CacheSize-- == 0) {
            WRITE_INDEX_REGISTER(pReadRegister, Read);
            CacheSize = QUEUE_BATCH_SIZE;
        }

        return TRUE;
    }

    BOOL WriteQueue(dword Reference)
    {
        dword* pQueueElement;

        /* The following code segment ensures the read index register
         * is not read too frequently. Thereby, minimizing
         * utilization of the PCI bus. */

        if (Headroom == 0) {
            /* Headroom was initialized to zero, and must be reinitialized
             * to a non-zero value in the following code segment before
             * the software is able to write a reference from the queue.
             * The Headroom is the free space in the queue when the
             * read index was last read by software, minus the number of
             * these locations that have been written. */
            Read = READ_INDEX_REGISTER(pReadRegister);
            if (Read < Write)
                  Headroom = Read - Start + End - Write;
            else
                  Headroom = Read - Write;
            /* Exit if the queue is full */
            if (Headroom == 0) return FALSE;
```

```
    }
    Headroom--;

    /* Write the reference to a RAM location */
    pQueueElement = pQueueBaseAddress + Write;
    *pQueueElement = Reference;

    /* Update the write index for next time.
     * Write is a post-increment operation */
    Write++;
    if (Write == End)
       Write = Start;

    /* The following code segment ensures the write index register
     * is not written too frequently. Thereby, minimizing
     * utilization of the PCI bus. */

    if (CacheSize-- == 0) {
       WRITE_INDEX_REGISTER(pWriteRegister, Write);
       CacheSize = QUEUE_BATCH_SIZE;
    }

    return TRUE;
}
```

An alternative method of reading from a queue is to poll a queue location in RAM, waiting for the FREEDM-84P672 to write a reference to the queue. This method is recommended when interrupts RPQRDYI and TDQFI are disabled, and processing of the RPDR Ready queue and the TDR Free queue must take place by polling. The following code illustrates this method.

```
#define INVALID_REFERENCE      0xFFFFFFFF

/* this routine assumes all empty queue locations were initialized
 * with the value 0xFFFFFFFF */

BOOL PollQueue(dword* pReference)
{
    dword* pQueueElement;

    /* Read the reference from a RAM location */
    pQueueElement = pQueueBaseAddress + NextReadLocation;
    *pReference = *pQueueElement;

    if (*pReference == INVALID_REFERENCE) {
       /* the queue location was not overwritten by the FREEDM-84P672, so
        * the reference is invalid, and PollQueue() does not return
        * a valid reference. */
```

```
            return FALSE;
         }
         else {
            /* the queue location was overwritten by the FREEDM-84P672, so
             * the reference is valid, proceed by overwriting the queue
             * location with an invalid reference. */
            *pQueueElement = INVALID_REFERENCE;

            /* write the FREEDM-84P672 register every n'th packet */
            if (CacheSize++ == QUEUE_BATCH_SIZE) {
                  WRITE_INDEX_REGISTER(pReadRegister, NextReadLocation);
                  CacheSize = 0;
            }

            /* calculate next read index since
             * read is a pre-increment operation */
            NextReadLocation++;
            if (NextReadLocation == End) {
                  NextReadLocation = Start;
            }
            return TRUE;
         }
      }
```

5 INTERRUPT ARCHITECTURE

This section provides an overview of the FREEDM-84P672 interrupt architecture. Detailed information on the individual interrupts is available in the Longform Datasheet[1].

5.1 Non-SBI Interrupts

The FREEDM-84P672 provides a number of individual interrupts which are identified as 'I' bits within the **FREEDM-84P672 Master Interrupt Status** (0x008) register. When an interrupt source becomes active, the 'I' bit is set and remains set until the **FREEDM-84P672 Master Interrupt Status** (0x008) register is read.

The FREEDM-84P672 provides interrupts to the PCI bus via the PCIINTB pin of the FREEDM-84P672. This signal is typically routed to an embedded processor via the INTA#, INTB#, INTC# or INTD# pin on the PCI bus. The PCIINTB pin is gated by the **FREEDM-84P672 Master Interrupt Enable** (0x004) register. This register contains 'E' bits which can mask the 'I' bit from causing an interrupt on the PCIINTB pin of the FREEDM-84P672. When the 'E' and 'I' bits of an interrupt source are both high, then the PCIINTB pin is active. When the 'E' bit is low, the interrupt source will not activate the PCIINTB pin, regardless of the 'I' bit status. However, the 'I' bit remains valid when interrupts are disabled and may be polled to detect the various events.

The complete list of 'I' bits and 'E' bits for non-SBI interrupts is shown below:

'E' Bit	'I' Bit	Description
SERRE	SERRI	System Error
PERRE	PERRI	Parity Error
RFCSEE	RFCSEI	Receive FCS Error
RABRTE	RABRTI	Receive Abort
RPFEE	RPFEI	Receive Packet Format Error
RFOVRE	RFOVRI	Receive FIFO Overrun Error
RPQSFE	RPQSFI	Small Buffer Cache Read
RPQLFE	RPQLFI	Large Buffer Cache Read
RPQRDYE	RPQRDYI	RPQR Ready Queue Write
RPDFQEE	RPDFQEI	RPDR Free Queue Error
RPDRQEE	RPDRQEI	RPDR Ready Queue Error
TDQFE	TDQFI	TDR Free Queue Write
TDQRDYE	TDQRDYI	TDR Ready Queue Read
TDFQEE	TDFQEI	TDR Free Queue Error
IOCE	IOCI	Interrupt On Complete

'E' Bit	'I' Bit	Description
TFUDRE	TFUDRI	Transmit FIFO Underflow Error

Interrupt Service Routine

The following code segment illustrates how interrupts for transmit and receive packets can be processed:

```
#define      RPQSFI                      0x0040
#define      RPQLFI                      0x0080
#define      RPQRDYI                     0x0100
#define      TDQFI                       0x0800
#define      IOCI                        0x4000
#define      RX_FREE_INTERRUPT           RPQLFI & RPQSFI
#define      TX_RX_INTERRUPT             TDQFI & IOCI & RPQRDYI
#define      READ_REGISTER(address)      ((*address)&0xFFFF)

/* read and clear the interrupt status */
Status == READ_REGISTER(pFreedmMasterInterruptStatusRegister);

if (Status&(TX_RX_INTERRUPT|RX_FREE_INTERRUPT)) {

    /* disable interrupts scheduled for deferred processing */
    Enable = READ_REGISTER(pFreedmMasterInterruptEnableRegister);

    /* disable active TX_RX_INTERRUPT bits */
    Enable &= ~TX_RX_INTERRUPT;
    WRITE_REGISTER(pFreedmMasterInterruptEnableRegister, Enable);

    /* Schedule processing of these interrupts within a
     * deferred processing routine. The deferred processing routine
     * should run after interrupt service routine, and with a lower
     * priority than the interrupt service routine. The deferred
     * processing routine must enable the relevant 'E' bits when it
     * is done with processing of Status values. */
    ScheduleDPR(Status);
}
```

Notes:

- The pseudo code shows how interrupt status bits are processed to pass control over to routines that do transmit and receive interrupt processing. The actual processing of receive packets and transmit packets must be interleaved to ensure that the host software does not continuously service

transmit packets while there are receive packets waiting to be serviced. This could lead to a receive FIFO overrun or a transmit FIFO underflow. By interleaving processing of the TD Free queue and the RPD Ready queue, the user can ensure that either queue will never be full, and that queue processing latencies are balanced among the transmit and receive paths.

- The pseudo code does not show how to process "critical error interrupts"; the list of these is shown in the table above. These interrupts must be processed in a manner analogous to the TX_RX_INTERRUPT bits shown in the pseudo code.

5.2 SBI Interrupts

In addition to the interrupts described in section 5.1, interrupts can be provided to the PCI bus by the SBI Extract block of the FREEDM-84P672.

The SBI Extracter interrupt status bit (SBIEXTI) of the **FREEDM-84P672 Master SBI Interrupt Status** (0x02C) register reports an error condition from the SBI Extract block to the PCI host. Reading this register acknowledges and clears the interrupt.

The SBI Extracter interrupt enable bit (SBIEXTE) of the **FREEDM-84P672 Master SBI Interrupt Enable** (0x028) register can mask the SBIEXTI bit from causing an interrupt on the PCIINTB pin. When the SBIEXTE and SBIEXTI pins are both high, then the PCIINTB pin is active. When the SBIEXTE is low, the interrupt source will not activate the PCIINTB pin, regardless of the SBIEXTI status. However, SBIEXTI remains valid when interrupts are disabled and may be polled to detect SBI Extract block error conditions.

SBI Extract Parity Error Interrupt

In the FREEDM-84P672, the only error condition which the SBI Extract block reports is a parity error on the SBI DROP BUS.

The PERRI bit of the **SBI EXTRACT Parity Error Interrupt Reason** (0x5DC) register indicates that an SBI parity error has been detected. Reading this register clears this bit. The TRIB[4:0] and SPE[1:0] fields of this register specify the SBI tributary for which a parity error was detected, and are only valid when PERRI is set.

The SBI_PERR_EN bit of the **SBI EXTRACT Control** (0x5C0) register enables or disables SBI Parity Error Interrupts. When SBI_PERR_EN is low, SBI Parity Error Interrupts are disabled. When SBI_PERR_EN is high, SBI Parity Error

Interrupts are enabled. In both cases, the **SBI EXTRACT Parity Error Interrupt Reason** (0x5DC) register is updated when a parity error occurs.

Note: Even if SBI_PERR_EN and PERRI are both high (causing SBIEXTI to report an error condition), SBIEXTE must also be high for the SBI Extract block to cause an interrupt on the PCIINTB pin.

6 PCI CONFIGURATION SPACE

The purpose of the PCI Configuration Space is to provide device specific information in a common template such that software can identify each PCI device in the system, determine the individual functions provided by each device and allocate system resources to each device. The software must also write bits to enable the FREEDM-84P672 to respond as a target to a PCI host master transaction. Please see section 12.1 for specific operational procedures and register values that must be modified.

6.1 Accessing the PCI Configuration Space

The FREEDM-84P672 responds to Type 0 configuration cycles for a single function device, as described in the PCI specification[2]. The FREEDM-84P672 only uses the IDSEL pin and the AD[1:0] = 00B to determine whether to respond to a configuration cycle. During the address phase of the configuration cycle, the AD[7:2] pins specify which of the 64 DWORD aligned Configuration Space registers is accessed. During the subsequent data phases, the BE#[3:0] pins specify which byte lanes within the 32-bit data bus are accessed.

The method of generating the configuration cycle is described in the PCI specification for a PC-AT compatible architecture, but for other system architectures, the method of generating configuration accesses is not defined in the PCI specification. The designer of the system must provide a mechanism that allows PCI configuration cycles to be generated by software. The designer must also specify an API to read and/or write registers within the Configuration Space.

6.2 PCI Configuration Registers

Portions of the PCI Configuration Space are mandatory in order for a PCI device to be in full compliance with the PCI specification. This section identifies the registers which are implemented in the FREEDM-84P672. The reader is referred to the PCI specification[2] and the Longform Datasheet[1] for an in-depth description of these registers.

The mandatory fields are listed below and shown in bold text in Figure 9.

- Vendor ID
- Device ID
- Command

- PCI Status
- Revision ID
- Class Code
- Header Type

Implementation of the other registers in a Type 0 Configuration Space is optional. Fields marked with asterisks (*) are not implemented in the FREEDM-84P672 Configuration Space. These fields will return 0 when read.

Figure 9 – FREEDM-84P672 Type 0 Configuration Space Header

DWORD Register	Address	Byte 3	Byte 2	Byte 1	Byte 0
1	0x00	**Device ID**		**Vendor ID**	
2	0x04	**Status**		**Command**	
3	0x08	**Class Code**			**Revision ID**
4	0x0C	BIST*	**Header Type**	Latency Timer	Cache Line Size
5	0x10	Base Address 0 (CBI Memory Address)			
6	0x14	Base Address 1*			
7	0x18	Base Address 2*			
8	0x1C	Base Address 3*			
9	0x20	Base Address 4*			
10	0x24	Base Address 5*			
11	0x28	Cardbus CIS Pointer*			
12	0x2C	Subsystem ID*		Subsystem Vendor ID*	
13	0x30	Expansion ROM Base Address*			
14	0x34	Reserved*			
15	0x38	Reserved*			
16	0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

7 CONFIGURING THE SBI INTERFACE

The Scaleable Bandwidth Interconnect (SBI) is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links of varying bandwidth. The bus is timed to a reference 19.44MHz clock and a 2kHz or 166.7Hz frame pulse. All sources and sinks of data on the bus are timed to the reference clock and frame pulse.

The SBI multiplexing structure is modeled on the SONET/SDH standards. The SONET/SDH virtual tributary structure is used to carry T1/J1 and E1 links. Unchannelised DS3 payloads follow a byte synchronous structure modeled on the SONET/SDH format.

The multiplexed links are separated into three Synchronous Payload Envelopes (SPEs). Each envelope may be configured independently to carry up to 28 T1/J1s, 21 E1s or a DS3.

Full details of the operation of the SBI interface are provided in the SBI Compatibility Specification [4].

7.1 Configuring the SBI DROP BUS

The SBI DROP BUS is a byte wide serial bus which drops SBI tributaries from multiple PHY devices to multiple link layer devices such as the FREEDM-84P672.

The SBI DROP BUS is configured by programming bits within the **FREEDM-84P672 SBI DROP BUS Master Configuration** (0x048) register. The default configuration is as follows:

Bit	Register	Value
SPE1_TYP[1:0]	**FREEDM-84P672 SBI DROP BUS Master Configuration** (0x048)	00
SPE2_TYP[1:0]	**FREEDM-84P672 SBI DROP BUS Master Configuration** (0x048)	00
SPE3_TYP[1:0]	**FREEDM-84P672 SBI DROP BUS Master Configuration** (0x048)	00
FCLK_FREQ[1:0]	**FREEDM-84P672 SBI DROP BUS Master Configuration** (0x048)	00
Reserved[1:0]	**FREEDM-84P672 SBI DROP BUS Master Configuration** (0x048)	00

The default indicates that all three Synchronous Payload Envelopes conveyed on the SBI DROP BUS are configured for 28 T1/J1 links and the FASTCLK input operates at a frequency of 51.84 MHz.

SPE Type on the SBI DROP BUS

The SPE type bits (SPEn_TYP[1:0]) determine the configuration of each of the three Synchronous Payload Envelopes conveyed on the SBI DROP BUS, according to the following table.

SPEn_TYP[1:0]	Link Configuration
00	28 T1/J1 links
01	21 E1 links
10	Single DS-3 link
11	Reserved

FASTCLK Frequency

The high-speed reference clock signal (FASTCLK) is used by the FREEDM-84P672 to generate an internal clock for use when processing DS-3 links. The FASTCLK frequency selector bits (FCLK_FREQ[1:0]) must be set according to the following table, depending on the frequency chosen for the FASTCLK input.

FCLK_FREQ[1:0]	FASTCLK Frequency
00	51.84 MHz
01	44.928 MHz
10	Reserved
11	66 MHz

7.2 Configuring the SBI ADD BUS

The SBI ADD BUS is a byte wide serial bus which aggregates TDM tributaries from multiple link layer devices such as the FREEDM-84P672 to multiple PHY devices.

The SBI ADD BUS is configured by programming bits within the **FREEDM-84P672 SBI ADD BUS Master Configuration** (0x04C) register. The default configuration is as follows:

Bit	Register	Value
SPE1_TYP[1:0]	**FREEDM-84P672 SBI ADD BUS Master Configuration** (0x04C)	00
SPE2_TYP[1:0]	**FREEDM-84P672 SBI ADD BUS Master Configuration** (0x04C)	00
SPE3_TYP[1:0]	**FREEDM-84P672 SBI ADD BUS Master Configuration** (0x04C)	00
FCLK_FREQ[1:0]	**FREEDM-84P672 SBI ADD BUS Master Configuration** (0x04C)	00
Reserved[4:0]	**FREEDM-84P672 SBI ADD BUS Master Configuration** (0x04C)	0x00
DEFAULT_DRV	**FREEDM-84P672 SBI ADD BUS Master Configuration** (0x04C)	0

The default indicates that all three Synchronous Payload Envelopes conveyed on the SBI ADD BUS are configured for 28 T1/J1 links, the FASTCLK input operates at a frequency of 51.84 MHz, and the FREEDM-84P672 will only drive the bus when it has data to send.

SPE Type on the SBI ADD BUS

The SPE type bits (SPEn_TYP[1:0]) determine the configuration of each of the three Synchronous Payload Envelopes conveyed on the SBI ADD BUS, according to the following table.

SPEn_TYP[1:0]	Link Configuration
00	28 T1/J1 links
01	21 E1 links
10	Single DS-3 link
11	Reserved

FASTCLK Frequency

The high-speed reference clock signal (FASTCLK) is used by the FREEDM-84P672 to generate an internal clock for use when processing DS-3 links. The FASTCLK frequency selector bits (FCLK_FREQ[1:0]) must be set according to the following table, depending on the frequency chosen for the FASTCLK input.

FCLK_FREQ[1:0]	FASTCLK Frequency
00	51.84 MHz
01	44.928 MHz
10	Reserved
11	66 MHz

Default Bus Driver

The Default Bus Driver selector bit (DEFAULT_DRV) enables the FREEDM-84P672 device to drive the SBI ADD BUS when no other device is doing so. It is recommended that one device connected to an SBI Bus be nominated as a default driver and configured to drive the bus when no other device is doing so (when the ADETECT[1:0] inputs are both 0). This feature is configured as follows:

DEFAULT_DRV	Function
0	The FREEDM-84P672 will only drive the bus when it has data to send (and when ADETECT[1:0] are both 0).
1	The FREEDM-84P672 will drive the bus whenever the ADETECT[1:0] inputs are both 0.

8 CONFIGURING THE SBI EXTRACTER AND INSERTER

8.1 Configuring the SBI Extracter

The SBI receive circuitry consists of an SBI Extract block and three SBI Parallel to Serial Converter (SBI PISO) blocks. The SBI Extract block receives data from the SBI DROP BUS and converts it to an internal parallel bus format. The received data is then converted to serial bit streams by the PISO blocks. Each PISO block processes one of the three Synchronous Payload Envelopes (SPEs) conveyed on the SBI DROP BUS.

The SBI Extract block may be configured to enable or disable reception of individual tributaries within the SBI DROP bus. Individual tributaries may also be configured to operate in framed or unframed mode.

Each PISO block inputs data related to one SPE from the internal parallel bus and generates either 28 serial data streams at T1/J1 rate, 21 streams at E1 rate or a single stream at DS-3 rate. These serial streams are then processed by the Receive Channel Assigner block.

8.1.1 SBI EXTRACT Control

The SBI Extract block is controlled by programming bits within the **SBI EXTRACT Control** (0x5C0) register. The default configuration is as follows:

Bit	Register	Value
SBI_PAR_CTL	**SBI EXTRACT Control** (0x5C0)	1
SBI_PERR_EN	**SBI EXTRACT Control** (0x5C0)	0
Reserved[2:0]	**SBI EXTRACT Control** (0x5C0)	000
Reserved[3]	**SBI EXTRACT Control** (0x5C0)	0

The default indicates that odd parity mode is used for checking the SBI parity signal, and that the SBI Parity Error interrupts are disabled.

SBI Parity Mode

The SBI_PAR_CTL bit is used to configure the Parity mode for checking of the SBI parity signal, DDP as follows:

SBI_PAR_CTL	Function
0	Even parity checking.
1	Odd parity checking.

SBI Parity Error Interrupt Enable

The SBI_PERR_EN bit is used to enable SBI parity error interrupt generation and is decoded in the following table. Please see section 5.2 for more information on the SBI parity error interrupt.

SBI_PERR_EN	Function
0	SBI parity error interrupts are disabled.
1	SBI parity error interrupts are enabled.

8.1.2 SBI EXTRACT Tributary Configuration

SBI EXTRACT tributary configuration information is read from and written to the SBI EXTRACT tributary control configuration RAM. An SBI tributary in the receive direction is configured using the following procedure:

1. Poll the BUSY bit of the **SBI EXTRACT Tributary RAM Indirect Access Control** (0x5D0) register until it is zero. This ensures that a previous indirect RAM access has completed and a new indirect RAM access can be started.

2. The TRIB[4:0] and SPE[1:0] fields of the **SBI EXTRACT Tributary RAM Indirect Access Address** (0x5CC) register are used to specify which SBI tributary the control configuration RAM write or read operation will apply to. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Write this register as follows:

Bit	Register	Value
TRIB[4:0]	**SBI EXTRACT Tributary RAM Indirect Access Address** (0x5CC)	See above
SPE[1:0]	**SBI EXTRACT Tributary RAM Indirect Access Address** (0x5CC)	See above
Reserved	**SBI EXTRACT Tributary RAM Indirect Access Address** (0x5CC)	0

3. The ENBL bit of the **SBI EXTRACT Tributary RAM Indirect Access Data** (0x5D8) register is used to enable the tributary. Writing to the tributary control configuration RAM with the ENBL bit set enables the SBI EXTRACT block to take tributary data from an SBI tributary and output that data to the SBI PISO blocks.

   The TRIB_TYP[1:0] field of the **SBI EXTRACT Tributary RAM Indirect Access Data** (0x5D8) register is used to configure the tributary to operate in framed or unframed mode as follows:

TRIB_TYP[1:0]	Tributary type
00	Reserved
01	Framed
10	Unframed
11	Reserved

   Specify the configuration data to be written to the tributary control configuration RAM by writing the following register:

Bit	Register	Value
ENBL	**SBI EXTRACT Tributary RAM Indirect Access Data** (0x5D8)	See above
Reserved[0]	**SBI EXTRACT Tributary RAM Indirect Access Data** (0x5D8)	0
TRIB_TYP[1:0]	**SBI EXTRACT Tributary RAM Indirect Access Data** (0x5D8)	See above
Reserved[3:1]	**SBI EXTRACT Tributary RAM Indirect Access Data** (0x5D8)	000

4. Trigger an indirect write operation on the tributary control configuration RAM by writing the following register:

Bit	Register	Value
Reserved	**SBI EXTRACT Tributary RAM Indirect Access Control** (0x5D0)	0
RWB	**SBI EXTRACT Tributary RAM Indirect Access Control** (0x5D0)	0
BUSY	**SBI EXTRACT Tributary RAM Indirect Access Control** (0x5D0)	X

8.2 Configuring the SBI Inserter

The SBI transmit circuitry consists of an SBI Insert block and three SBI Serial to Parallel Converter (SBI SIPO) blocks. Each SIPO block processes data for one of the three Synchronous Payload Envelopes (SPEs) conveyed on the SBI ADD BUS. It receives serial data on either 28 links running at T1/J1 rate, 21 links at E1 rate or a single link at DS-3 rate and converts it to an internal parallel bus format. The SBI Insert block receives data from the SIPO blocks in the internal format and transmits it on the SBI ADD BUS.

The SIPO blocks generate the serial clocks for the TCAS672 and thus are able to control the rate at which data is transmitted on to the SBI. The SBI Insert block can command the SIPO blocks to speed up or slow down these clocks in response to justification requests received on the SBI interface. This feature is controlled by the CLK_MSTR bit which is explained in section 8.2.2. The SBI Insert block also contains FIFO circuitry to compensate for short term variations in the rate at which data is output by the TCAS672 and the rate at which it is transmitted on the SBI ADD BUS.

The SBI Insert block may be configured to enable or disable transmission of individual tributaries on to the SBI ADD bus. Individual tributaries may also be configured to operate in framed or unframed mode.

8.2.1 SBI INSERT Control

The SBI Insert block is controlled by programming bits within the **SBI INSERT Control** (0x680) register. The default configuration is as follows:

Bit	Register	Value
SBI_PAR_CTL	**SBI INSERT Control** (0x680)	1
Reserved[2:0]	**SBI INSERT Control** (0x680)	000
Reserved[3]	**SBI INSERT Control** (0x680)	0

The default indicates that the odd parity mode is used for generating the SBI parity signal.

SBI Parity Mode

The SBI_PAR_CTL bit is used to configure the Parity mode for generation of the SBI parity signal, ADP as follows:

SBI_PAR_CTL	Function
0	Even parity generation.
1	Odd parity generation.

8.2.2 SBI INSERT Tributary Configuration

SBI INSERT tributary configuration information is read from and written to the SBI INSERT tributary control configuration RAM. An SBI tributary in the transmit direction is configured using the following procedure:

1. Poll the BUSY bit of the **SBI INSERT Tributary RAM Indirect Access Control** (0x690) register until it is zero. This ensures that a previous indirect RAM access has completed and a new indirect RAM access can be started.

2. The TRIB[4:0] and SPE[1:0] fields of the **SBI INSERT Tributary RAM Indirect Access Address** (0x68C) register are used to specify which SBI tributary the control configuration RAM write or read operation will apply to. Legal values for TRIB[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. Write this register as follows:

Bit	Register	Value
TRIB[4:0]	**SBI INSERT Tributary RAM Indirect Access Address** (0x68C)	See above
SPE[1:0]	**SBI INSERT Tributary RAM Indirect Access Address** (0x68C)	See above
Reserved	**SBI INSERT Tributary RAM Indirect Access Address** (0x68C)	0

3. The ENBL bit of the **SBI INSERT Tributary RAM Indirect Access Data** (0x698) register is used to enable the tributary. Writing to the tributary control configuration RAM with the ENBL bit set enables the SBI INSERT block to output tributary data on an SBI tributary.

   The TRIB_TYP[1:0] field of the **SBI INSERT Tributary RAM Indirect Access Data** (0x698) register is used to configure the tributary to operate in framed or unframed mode as follows:

TRIB_TYP[1:0]	Tributary type
00	Reserved
01	Framed
10	Unframed
11	Reserved

The CLK_MSTR bit of the **SBI INSERT Tributary RAM Indirect Access Data** (0x698) register configures the SBI tributary to operate as a timing master or slave. Setting CLK_MSTR to 1 configures the tributary as a timing master (AJUST_REQ input ignored). Setting CLK_MSTR to 0 configures the tributary as a timing slave (requests on AJUST_REQ honoured).

Specify the configuration data to be written to the tributary control configuration RAM by writing the following register:

Bit	Register	Value
ENBL	**SBI INSERT Tributary RAM Indirect Access Data** (0x698)	See above
Reserved	**SBI INSERT Tributary RAM Indirect Access Data** (0x698)	0
TRIB_TYP[1:0]	**SBI INSERT Tributary RAM Indirect Access Data** (0x698)	See above
CLK_MSTR	**SBI INSERT Tributary RAM Indirect Access Data** (0x698)	See above

4. Trigger an indirect write operation on the tributary control configuration RAM by writing the following register:

Bit	Register	Value
Reserved	**SBI INSERT Tributary RAM Indirect Access Control** (0x690)	0
RWB	**SBI INSERT Tributary RAM Indirect Access Control** (0x690)	0
BUSY	**SBI INSERT Tributary RAM Indirect Access Control** (0x690)	X

9 CONFIGURING THE SERIAL LINKS

Each of the 84 bi-directional links is controlled via the RCAS672 and the TCAS672 blocks of the FREEDM-84P672. The RCAS672 controls the receive data stream while the TCAS672 controls the transmit data stream.

The Receive Channel Assigner (RCAS672)

The Receive Channel Assigner block processes up to 84 serial links. When receiving data from the SBI PISO blocks, links may be configured to support channelised T1/J1/E1 traffic, unchannelised DS-3 traffic or unframed traffic at T1/J1, E1 or DS-3 rates. When receiving data from the RCLK/RD inputs, links 0, 1 and 2 support unchannelised data at arbitary rates up to 52 Mbps.

Each link is independent and has its own associated clock. For each link, the RCAS672 performs a serial to parallel conversion to form data bytes. The data bytes are multiplexed, in byte serial format, for delivery to the Receive HDLC Processor / Partial Packet Buffer block (RHDL672) at SYSCLK rate. In the event where multiple streams have accumulated a byte of data, multiplexing is performed on a fixed priority basis with link #0 having the highest priority and link #83 the lowest.

The 84 RCAS links have a fixed relationship to the SPE and tributary numbers on the SBI DROP BUS as shown in the following table.

SBI SPE No.	SBI Trib. No.	RCAS Link No.	SBI SPE No.	SBI Trib. No.	RCAS Link No.	SBI SPE No.	SBI Trib. No.	RCAS Link No.
1	1	0	2	1	1	3	1	2
1	2	3	2	2	4	3	2	5
1	3	6	2	3	7	3	3	8
1	4	9	2	4	10	3	4	11
1	5	12	2	5	13	3	5	14
1	6	15	2	6	16	3	6	17
1	7	18	2	7	19	3	7	20
1	8	21	2	8	22	3	8	23
1	9	24	2	9	25	3	9	26
1	10	27	2	10	28	3	10	29

SBI SPE No.	SBI Trib. No.	RCAS Link No.	SBI SPE No.	SBI Trib. No.	RCAS Link No.	SBI SPE No.	SBI Trib. No.	RCAS Link No.
1	11	30	2	11	31	3	11	32
1	12	33	2	12	34	3	12	35
1	13	36	2	13	37	3	13	38
1	14	39	2	14	40	3	14	41
1	15	42	2	15	43	3	15	44
1	16	45	2	16	46	3	16	47
1	17	48	2	17	49	3	17	50
1	18	51	2	18	52	3	18	53
1	19	54	2	19	55	3	19	56
1	20	57	2	20	58	3	20	59
1	21	60	2	21	61	3	21	62
1	22	63	2	22	64	3	22	65
1	23	66	2	23	67	3	23	68
1	24	69	2	24	70	3	24	71
1	25	72	2	25	73	3	25	74
1	26	75	2	26	76	3	26	77
1	27	78	2	27	79	3	27	80
1	28	81	2	28	82	3	28	83

Links containing a T1/J1 or an E1 stream may be channelised. Data at each time-slot may be independently assigned to a different channel. The RCAS672 performs a table lookup to associate the link and time-slot identity with a channel. The position of T1/J1 and E1 framing bits/bytes is identified by frame pulse signals generated by the SBI PISO blocks. Links containing a DS-3 stream are unchannelised, i.e. all data on the link belongs to one channel. The RCAS672 performs a table lookup using only the link number to determine the associated channel, as time-slots are non-existent in unchannelised links. Links may additionally be configured to operate in an unframed "clear channel" mode, in which all bit positions, including those normally reserved for framing information, are assumed to be carrying HDLC data. Links configured in unframed mode operate as unchannelised regardless of link rate and the

RCAS672 performs a table lookup using only the link number to determine the associated channel.

The Transmit Channel Assigner (TCAS672)

The Transmit Channel Assigner block processes up to 672 channels. Data for all channels is sourced from a single byte-serial stream from the Transmit HDLC Controller / Partial Packet Buffer block (THDL672). The TCAS672 demultiplexes the data and assigns each byte to any one of 84 links. When sending data to the SBI SIPO blocks, each link may be configured to support channelised T1/J1/E1 traffic, unchannelised DS-3 traffic or unframed traffic at T1/J1, E1 or DS-3 rates. When sending data to the TD outputs, links 0, 1 and 2 support unchannelised data at arbitary rates up to 52 Mbps. Each link is independent and has its own associated clock.

The 84 TCAS links have a fixed relationship to the SPE and tributary numbers on the SBI ADD BUS as shown in the following table.

SBI SPE No.	SBI Trib. No.	TCAS Link No.	SBI SPE No.	SBI Trib. No.	TCAS Link No.	SBI SPE No.	SBI Trib. No.	TCAS Link No.
1	1	0	2	1	1	3	1	2
1	2	3	2	2	4	3	2	5
1	3	6	2	3	7	3	3	8
1	4	9	2	4	10	3	4	11
1	5	12	2	5	13	3	5	14
1	6	15	2	6	16	3	6	17
1	7	18	2	7	19	3	7	20
1	8	21	2	8	22	3	8	23
1	9	24	2	9	25	3	9	26
1	10	27	2	10	28	3	10	29
1	11	30	2	11	31	3	11	32
1	12	33	2	12	34	3	12	35
1	13	36	2	13	37	3	13	38
1	14	39	2	14	40	3	14	41
1	15	42	2	15	43	3	15	44
1	16	45	2	16	46	3	16	47

SBI SPE No.	SBI Trib. No.	TCAS Link No.	SBI SPE No.	SBI Trib. No.	TCAS Link No.	SBI SPE No.	SBI Trib. No.	TCAS Link No.
1	17	48	2	17	49	3	17	50
1	18	51	2	18	52	3	18	53
1	19	54	2	19	55	3	19	56
1	20	57	2	20	58	3	20	59
1	21	60	2	21	61	3	21	62
1	22	63	2	22	64	3	22	65
1	23	66	2	23	67	3	23	68
1	24	69	2	24	70	3	24	71
1	25	72	2	25	73	3	25	74
1	26	75	2	26	76	3	26	77
1	27	78	2	27	79	3	27	80
1	28	81	2	28	82	3	28	83

As shown in the table above, TCAS links 0, 1, and 2 are mapped to tributary 1 of SPEs 1, 2 and 3 respectively. These links may be configured to operate at DS-3 rate. (They may also be configured to output data to the TD outputs at rates up to 52 Mbps.) For each of these high-speed links, the TCAS672 provides a six byte FIFO. For the remaining links (TCAS links 3 to 83, mapped to links 2 to 28 of each SPE), the TCAS672 provides a single byte holding register. The TCAS672 performs parallel to serial conversion to form bit-serial streams which are passed to the SBI SIPO blocks. In the event where multiple links are in need of data, TCAS672 requests data from upstream blocks on a fixed priority basis with link 0 having the highest priority and link 83 the lowest.

Links containing a T1/J1 or an E1 stream may be channelised. Data at each time-slot may be independently assigned to be sourced from a different channel. The position of T1/J1 and E1 framing bits/bytes is identified by frame pulse signals generated by the SBI SIPO blocks. With knowledge of the transmit link and time-slot identity, the TCAS672 performs a table look-up to identify the channel from which a data byte is to be sourced.

Links containing a DS-3 stream are unchannelised, in which case, all data bytes on the link belong to one channel. The TCAS672 performs a table look-up to identify the channel to which a data byte belongs using only the outgoing link identity, as no time-slots are associated with unchannelised links. Links may

additionally be configured to operate in an unframed "clear channel" mode, in which case the FREEDM-84P672 will output HDLC data in all bit positions, including those normally reserved for framing information. Links configured in unframed mode operate as unchannelised regardless of link rate and the TCAS672 performs a table lookup using only the link number to determine the associated channel.

9.1 SBI SPE/Tributary Links

When the SPEn_EN input pin is high, the corresponding Synchronous Payload Envelope conveyed on the SBI interface is enabled and the corresponding independently timed link is disabled. This section describes the configuration of the operational and framing modes of those links mapped to SPEs on the SBI DROP and ADD buses.

SBI Mode for SPEn Links

The SBI mode select bits (SBI_MODE[2:0]) in the following registers configure the receive and transmit links of SPEn, where $1 \leq n \leq 3$:

Bit	SPE No.	Register
SBI_MODE[2:0]	1	**RCAS SBI SPE1 Configuration Register #1** (0x140)
SBI_MODE[2:0]	2	**RCAS SBI SPE2 Configuration Register #1** (0x148)
SBI_MODE[2:0]	3	**RCAS SBI SPE3 Configuration Register #1** (0x150)
SBI_MODE[2:0]	1	**TCAS SBI SPE1 Configuration Register #1** (0x440)
SBI_MODE[2:0]	2	**TCAS SBI SPE2 Configuration Register #1** (0x448)
SBI_MODE[2:0]	3	**TCAS SBI SPE3 Configuration Register #1** (0x450)

The encoding of the SBI_MODE[2:0] bits is shown in the following table, where $1 \leq n \leq 3$:

SBI_MODE [2:0]	SPEn Configuration
000	Single unchannelised DS-3 on link n–1
001	28 T1/J1 links
010	21 E1 links (links corresponding to SPEn tributaries 22-28 are unused)
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

Framing Mode for SPEn Links

The framing mode of those links mapped to SPE 1 of the SBI DROP BUS is configured using the FEN[11:0] bits of the **RCAS SBI SPE1 Configuration Register #1** (0x140) and the FEN[27:12] bits of the **RCAS SBI SPE1 Configuration Register #2** (0x144). Each FEN bit, FEN[n], configures link 3n for framed operation. In unframed operation (FEN[n] = 0), all framing bit locations are treated as containing data. In framed mode (FEN[n] = 1), the contents of framing bit locations are ignored.

The framing mode of those links mapped to SPE 2 of the SBI DROP BUS is configured using the FEN[11:0] bits of the **RCAS SBI SPE2 Configuration Register #1** (0x148) and the FEN[27:12] bits of the **RCAS SBI SPE2 Configuration Register #2** (0x14C). Each FEN bit, FEN[n], configures link 3n+1 for framed operation. In unframed operation (FEN[n] = 0), all framing bit locations are treated as containing data. In framed mode (FEN[n] = 1), the contents of framing bit locations are ignored.

The framing mode of those links mapped to SPE 3 of the SBI DROP BUS is configured using the FEN[11:0] bits of the **RCAS SBI SPE3 Configuration Register #1** (0x150) and the FEN[27:12] bits of the **RCAS SBI SPE3 Configuration Register #2** (0x154). Each FEN bit, FEN[n], configures link 3n+2 for framed operation. In unframed operation (FEN[n] = 0), all framing bit locations are treated as containing data. In framed mode (FEN[n] = 1), the contents of framing bit locations are ignored.

The framing mode of those links mapped to SPE 1 of the SBI ADD BUS is configured using the FEN[11:0] bits of the **TCAS SBI SPE1 Configuration Register #1** (0x440) and the FEN[27:12] bits of the **TCAS SBI SPE1 Configuration Register #2** (0x444). Each FEN bit, FEN[n], configures link 3n for framed operation. In unframed operation (FEN[n] = 0), HDLC data is

transmitted in all framing bit locations. In framed mode (FEN[n] = 1), the framing bit locations are unused.

The framing mode of those links mapped to SPE 2 of the SBI ADD BUS is configured using the FEN[11:0] bits of the **TCAS SBI SPE2 Configuration Register #1** (0x448) and the FEN[27:12] bits of the **TCAS SBI SPE2 Configuration Register #2** (0x44C). Each FEN bit, FEN[n], configures link 3n+1 for framed operation. In unframed operation (FEN[n] = 0), HDLC data is transmitted in all framing bit locations. In framed mode (FEN[n] = 1), the framing bit locations are unused.

The framing mode of those links mapped to SPE 3 of the SBI ADD BUS is configured using the FEN[11:0] bits of the **TCAS SBI SPE3 Configuration Register #1** (0x450) and the FEN[27:12] bits of the **TCAS SBI SPE3 Configuration Register #2** (0x454). Each FEN bit, FEN[n], configures link 3n+2 for framed operation. In unframed operation (FEN[n] = 0), HDLC data is transmitted in all framing bit locations. In framed mode (FEN[n] = 1), the framing bit locations are unused.

Idle Time-Slot Fill Data

The fill data bits (FDATA[7:0]) of the **TCAS Idle Time-slot Fill Data** (0x40C) register are transmitted during disabled time-slots of a channelised link (when the PROV bit of the **TCAS Indirect Channel Data** (0x404) register is low). The default value of FDATA[7:0] is 0xFF.

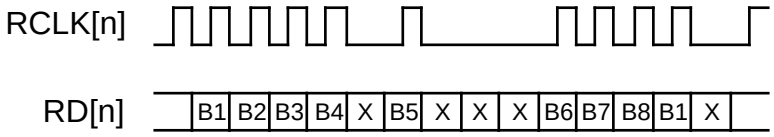
9.2 Clock/Data Links

When the SPEn_EN input pin is low, the corresponding Synchronous Payload Envelope conveyed on the SBI interface is unused and the corresponding independently timed link (signals RCLK[n-1], RD[n-1], TCLK[n-1] and TD[n-1]) is enabled, where $1 \leq n \leq 3$.

The timing relationship of the receive clock (RCLK[n]) and data (RD[n]) signals is shown in Figure 10, where $0 \leq n \leq 2$. The receive data is viewed as a contiguous serial stream. There is no concept of time-slots or framing. Every eight bits are grouped together into a byte with arbitrary alignment. The first bit received (B1 in Figure 10) is deemed the most significant bit of an octet. The last bit received (B8) is deemed the least significant bit. Bits that are to be processed by the FREEDM-84P672 are clocked in on the rising edge of RCLK[n]. Bits that should be ignored (X in Figure 10) are squelched by holding RCLK[n] quiescent. In Figure 10, the quiescent period is shown to be a low level on RCLK[n]. A high level, effected by extending the high phase of the previous valid bit, is also

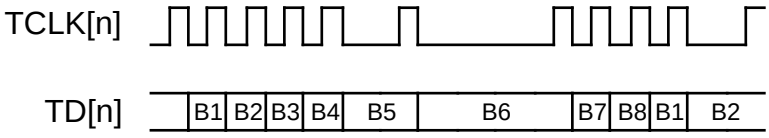
acceptable. Selection of bits for processing is arbitrary and is not subject to any byte alignment nor frame boundary considerations.

Figure 10 – Receive Link Timing



The timing relationship of the transmit clock (TCLK[n]) and data (TD[n]) signals is shown in Figure 11, where $0 \leq n \leq 2$. The transmit data is viewed as a contiguous serial stream. There is no concept of time-slots or framing. Every eight bits are grouped together into a byte with arbitrary byte alignment. Octet data is transmitted from most significant bit (B1 in Figure 11) and ending with the least significant bit (B8 in Figure 11). Bits are updated on the falling edge of TCLK[n]. A transmit link may be stalled by holding the corresponding TCLK[n] quiescent. In Figure 11, bits B5 and B2 are shown to be stalled for one cycle while bit B6 is shown to be stalled for three cycles. In Figure 11, the quiescent period is shown to be a low level on TCLK[n]. A high level, effected by extending the high phase of the previous valid bit, is also acceptable. Gapping of TCLK[n] can occur arbitrarily without regard to byte nor frame boundaries.

Figure 11 – Transmit Link Timing



The following registers control the operation of receive links #0 to #2 when they are configured to receive data from the RD[2:0] inputs (i.e. the corresponding SPEn_EN input pin is low). Since the only mode of operation of the clock/data links is unchannelised mode, no additional configuration is necessary. However, the programmer must ensure that the reserved bits in the following RCAS672 and TCAS672 registers are set low for correct operation of the FREEDM-84P672.

Bit	Register	Value
Reserved[2:0]	**RCAS Links #0 to #2 Configuration** (0x180 – 0x188)	000
Reserved[3]	**RCAS Links #0 to #2 Configuration** (0x180 – 0x188)	0

Bit	Register	Value
Reserved[2:0]	**TCAS Links #0 to #2 Configuration** (0x480 – 0x488)	000
Reserved[3]	**TCAS Links #0 to #2 Configuration** (0x480 – 0x488)	0

10 CONFIGURING THE PCI INTERFACE

Configuration of the PCI interface involves initialization of data structures, which is covered in section 4, and mapping of the Normal Mode Register Space, which is covered in section 12.1. This section covers configuration and control of the DMA activities. These are accessible within the RMAC672, TMAC672 and GPIC672 block registers.

10.1 Configuring the Receive DMA Controller (RMAC672)

The RMAC672 is the DMA controller which writes receive data into packet memory. It sources data from the RHDL672 and requests the GPIC672 to write the data across the PCI bus and into packet memory.

The RMAC672 is configured by programming bits within the **RMAC Control** (0x280) register. The values programmed affect all receive channels. The default configuration is as follows:

Bit	Register	Value
ENABLE	**RMAC Control** (0x280)	0
LCACHE	**RMAC Control** (0x280)	1
SCACHE	**RMAC Control** (0x280)	1
RAWMAX[1:0]	**RMAC Control** (0x280)	11
RPQ_RDYN[2:0]	**RMAC Control** (0x280)	000
RPQ_LFN[1:0]	**RMAC Control** (0x280)	00
RP1_SFN[1:0]	**RMAC Control** (0x280)	00
Reserved	**RMAC Control** (0x280)	0

The default indicates that the RMAC672 is disabled from DMA'ing receive data into packet memory.

Activation of the RMAC672

By default, the RMAC672 is disabled from DMA'ing receive data into packet memory. The ENABLE bit must be set to allow DMA of receive data into packet memory. The encoding of this bit is:

ENABLE	Function
0	The RMAC672 does not accept data from the RHDL672 and does not write data to host memory
1	The RMAC672 accepts data from the RHDL672 and writes it to host memory.

Free Buffer Cache Enable

The FREEDM-84P672 reads from packet memory to obtain unused receive buffers, and stores them in a cache if caching is enabled. The access can read just one RPDR, or six RPDR's if the cache is enabled. There is a separate cache for the small buffers and the large buffers; they can be individually enabled.

LCACHE (or SCACHE)	Function
0	The RMAC672 reads just one RPDR at a time.
1	The RMAC672 reads up to six RPDR's and stores them in a cache.

Raw Data Notification

The RAWMAX[1:0] field determines notification of receive occurrences. This field only applies to channels that are provisioned with the DELIN bit set low within the **RHDL Indirect Channel Data Register #1** (0x204) register. When the unprocessed data fills RAWMAX[1:0] + 1 buffers, the resulting buffer chain is placed in the RPDR Ready queue.

RPQRDYI, RPQLFI and RPQSFI Interrupt Frequency

The RPQ_RDYN[2:0] field indicates the number of RPDR's written to the RPDR Ready queue by the FREEDM-84P672 before an RPQRDYI interrupt is asserted. It essentially controls the frequency of RPQRDYI interrupts. When this interrupt occurs the software must process the linked list of buffers for each RPDR (packet) that is read from the RPDR Ready queue. Valid values are:

RPQ_RDYN[2:0]	No of RPDRs
000	1
001	4
010	6
011	8
100	16
101	32
110	Reserved
111	Reserved

The RPQ_LFN[1:0] field sets the number of times that a block of RPDR's are read from the Large Buffer Free Queue to the RMAC672's internal cache before the RPDR Large Buffer Free Queue interrupt (RPQLFI) is asserted. It essentially controls the frequency of RPQLFI interrupts. When this interrupt occurs the software must replenish the RPDRF Large queue with large buffers. Valid values are:

RPQ_LFN[1:0]	No of Reads
00	1
01	4
10	8
11	Reserved

The RPQ_SFN[1:0] field sets the number of times that a block of RPDR's are read from the Small Buffer Free Queue to the RMAC672's internal cache before the RPDR Small Buffer Free Queue interrupt (RPQSFI) is asserted. It essentially controls the frequency of RPQSFI interrupts. When this interrupt occurs the software must replenish the RPDRF Small queue with small buffers. Valid values are:

RPQ_SFN[1:0]	No of Reads
00	1
01	4

RPQ_SFN[1:0]	No of Reads
10	8
11	Reserved

10.2 Configuring the Transmit DMA Controller (TMAC672)

The TMAC672 is the DMA controller which reads transmit data from packet memory. It reads TDRs from the TDR Ready queue to determine the transmit buffer data which must be DMA'd across the PCI bus and passed onto the THDL672 block.

The TMAC672 is configured by programming bits within the **TMAC Control** (0x300) register. The values programmed affect all transmit channels. The default configuration is as follows:

Bit	Register	Value
ENABLE	**TMAC Control** (0x300)	0
CACHE	**TMAC Control** (0x300)	1
TDQ_RDYN[2:0]	**TMAC Control** (0x300)	000
TDQ_FRN[1:0]	**TMAC Control** (0x300)	00
FQFLUSH	**TMAC Control** (0x300)	0

The default indicates that the TMAC672 is disabled from DMA'ing transmit data from packet memory.

Activation of the TMAC672

By default, the TMAC672 is disabled from DMA'ing data from packet memory. The ENABLE bit must be set to allow DMA of transmit data. The encoding of this bit is:

ENABLE	Function
0	The TMAC672 does not read the TDR Ready queue in packet memory to transmit new packets. Once all linked lists of TD's built up by the TMAC672 have been exhausted, no more data will be transmitted on the TD[31:0] links.
1	The TMAC672 can read the TDR Ready queue in packet memory to transmit new packets.

Free Buffer Cache Enable

The CACHE enable bit allows the TMAC672 to cache up to six TDRs before writing them to the TDR Free queue.

CACHE	Function
0	The TMAC672 writes one TDR at a time to the TDR Free queue.
1	The TMAC672 caches up to six TDRs and writes them to the TDR Free queue at one time.

TDQRDYI and TDQFI Interrupt Frequency

The TDQ_RDYN[2:0] field indicates the number of TDRs read from the TDR Ready queue by the FREEDM-84P672 before an TDQRDYI interrupt is asserted. It essentially controls the frequency of TDQRDYI interrupts. Valid values are:

TDQ_RDYN[2:0]	No of TDRs
000	1
001	4
010	6
011	8
100	16
101	32
110	Reserved
111	Reserved

The TDQ_FRN[1:0] field sets the number of times that a block of TDRs are written to the TDR Free Queue to the TMAC672's internal cache before the TDR Free Queue interrupt (TDQFI) is asserted. It essentially controls the frequency of TDQFI interrupts. When this interrupt occurs the software must collect each TDR that is read from the TDR Free queue in order to confirm that a transmit packet was transmitted, so that the buffers can be reused. Valid values are:

TDQ_FRN[1:0]	No of Reads
00	1
01	4
10	8
11	Reserved

Free Queue Flush

The Free Queue Flush bit (FQFLUSH) may be used to initiate a dump of the free queue cache retained locally within the TMAC672 to the free queue located in PCI host memory. The FQFLUSH bit is self-clearing and will reset to zero when the flush is complete.

FQ_FLUSH	Function
0	No effect.
1	The TMAC672 dumps the contents of the free queue cache to the free queue in PCI host memory.

10.3 Configuring the General-Purpose PCI Controller (GPIC672)

The GPIC672 provides the interface to a 32-bit PCI bus operating at up to 66 MHz and bridges between the timing domain of the DMA controllers (specified by SYSCLK pin) and the timing domain of the PCI bus (specified by PCICLK pin). All transactions on the PCI bus that are initiated by the RMAC672 or TMAC672 are translated into PCI bus activity by the GPIC672. Except for the PCI Configuration Space registers and parity checking, the GPIC672 does not perform operations on the PCI bus data.

The GPIC672 is configured by programming bits within the **GPIC Control** (0x080) register. The default configuration is as follows:

Bit	Register	Value
Reserved	**GPIC Control** (0x080)	0
LENDIAN	**GPIC Control** (0x080)	1
SOE_E	**GPIC Control** (0x080)	0
PONS_E	**GPIC Control** (0x080)	0
RPWTH[5:0]	**GPIC Control** (0x080)	00 0000B

Little Endian Mode Bit

The LENDIAN bit controls the format of buffer data read from or written to packet memory. By default, the LENDIAN mode bit is set indicating Little Endian format. The Little Endian and Big Endian formats are described in Figures 12 and 13. The encoding of this bit is:

LENDIAN	Function
0	Buffer data is in Big Endian format.
1	Buffer data is in Little Endian format.

Figure 12 – Little Endian Format

		Bit 31 24	23 16	15 8	7 Bit 0
DWORD	00	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Address	04	BYTE 7	BYTE 6	BYTE 5	BYTE 4
		•	•	•	•
		•	•	•	•
		•	•	•	•
	n-4	BYTE n-1	BYTE n-2	BYTE n-3	BYTE n-4

Figure 13 – Big Endian Format

		Bit 31 24	23 16	15 8	7 Bit 0
DWORD	00	BYTE 0	BYTE 1	BYTE 2	BYTE 3
Address	04	BYTE 4	BYTE 5	BYTE 6	BYTE 7
		•	•	•	•
		•	•	•	•
		•	•	•	•
	n-4	BYTE n-4	BYTE n-3	BYTE n-2	BYTE n-1

Notes:

- Since the LENDIAN bit only controls the format of the buffer data, all of the control data structures such as queue elements, descriptors and descriptor references must be in Little Endian format.

- For Big Endian addressing memory, byte swapping is usually done by the host CPU, the PCI bridge or the software.

The SOE_E and PONS_E Bits

The stop on error enable (SOE_E) and the report PERR on SERR enable (PONS_E) are described in the Longform Datasheet[1]. These correspond to faults detected at the hardware level by the PCI bus interface.

Threshold for Early Bus Arbitration

The Receive Packet Write Threshold bits (RPWTH[5:0]) control early arbitration for the PCI bus. For non-zero values of RPWTH[5:0], the GPIC672 will begin requesting access to the PCI bus when the number of dwords of packet data loaded by the RMAC672 reaches the threshold specified by RPWTH[5:0]. When the Receive Packet Write Threshold is set to zero, the GPIC672 will begin requesting access to the PCI bus shortly after data starts to be loaded by the RMAC672. Non-zero values are usually used when SYSCLK runs slower than PCICLK.

11 HDLC AND CHANNEL FIFO CONFIGURATION

The FREEDM-84P672 processes the data stream in the receive direction via the RHDL672 block and it processes the data stream in the transmit direction via the THDL672 block. Each of these blocks must be configured via the Normal Mode Register Space.

11.1 Configuring the RHDL672

The RHDL672 is configured by programming bits within the **RHDL Configuration** (0x220) register and the **RHDL Maximum Packet Length** (0x224) register. The values programmed affect all receive channels. The default configuration is as follows:

Bit	Register	Value
LENCHK	**RHDL Configuration** (0x220)	0
TSTD	**RHDL Configuration** (0x220)	0
MAX[15:0]	**RHDL Maximum Packet Length** (0x224)	0xFFFF

The default indicates no maximum packet length checking and datacom bit ordering.

Maximum Packet Length

The RHDL672 may be configured to abort packets which exceed the maximum length of *n* where $0 \leq n \leq 0xFFFF$. The following bits are written to enable or disable this feature:

LENCHK	MAX[15:0]	Function
0	0xFFFF	Receive packets are not checked for maximum size and MAX[15:0] must be set to 0xFFFF.
1	n	Receive packets with total length, including address, control, information and FCS fields, greater than MAX[15:0] bytes are aborted and the remainder of the frame discarded.

Datacom/Telecom Bit Order

The RHDL672 may be configured to reverse the order of bits within a data byte of a write access on the PCI bus. The following bit is written to specify the order of bits:

TSTD	Function
0	Datacom standard: least significant bit of each byte on the PCI bus (AD[0], AD[8], AD[16], AD[24]) is the first HDLC bit received. Normally, when HDLC processing is enabled, the TSTD bit must be set to zero.
1	Telecom standard: most significant bit of each byte on the PCI bus (AD[7], AD[15], AD[23], AD[31]) is the first HDLC bit received.

11.2 Configuring the THDL672

The THDL672 is configured by programming bits within the **THDL Configuration** (0x3B0) register. The values programmed affect all transmit channels. The default configuration is as follows:

Bit	Register	Value
BURST[3:0]	**THDL Configuration** (0x3B0)	0000B
BURSTEN	**THDL Configuration** (0x3B0)	0
TSTD	**THDL Configuration** (0x3B0)	0
BIT8	**THDL Configuration** (0x3B0)	0

The default indicates PCI DMA transfer size is controlled by XFER[3:0] and data is formatted in datacom bit ordering.

Enabling Burst DMA Transfer

The burst length enable bit (BURSTEN) controls the use of BURST[3:0] in determining the amount of data requested in a single DMA transaction for channels whose channel transfer size is set to one block (XFER[3:0] = 0000B). BURSTEN has no effect on channels configured with other transfer sizes. The following bits are written to enable or disable this feature:

BURSTEN	BURST[3:0]	Function
0	X	The amount of data in a DMA transfer is limited to one block.
1	0 through 15 are valid	The THDL672 may combine several channel transfer size amounts into a single transaction. BURST[3:0] defines the maximum number of 16 byte blocks, less one, that is transferred in each DMA transaction. Thus, the minimum number of blocks is one (16 bytes) and the maximum is sixteen (256 bytes).

Datacom/Telecom Bit Order

The THDL672 may be configured to reverse the order of bits within a data byte of a read access on the PCI bus. The following bit is written to specify the order of bits:

TSTD	Function
0	Datacom standard: least significant bit of each byte on the PCI bus (AD[0], AD[8], AD[16], AD[24]) is the first HDLC bit transmitted. Normally, when HDLC processing is enabled, the TSTD bit must be set to zero.
1	Telecom standard: most significant bit of each byte on the PCI bus (AD[7], AD[15], AD[23], AD[31]) is the first HDLC bit transmitted.

BIT8

The BIT8 field affects channels of the THDL672 that are configured with 7BIT set. The BIT8 value specifies the data bit transmitted on the least significant bit of each octet.

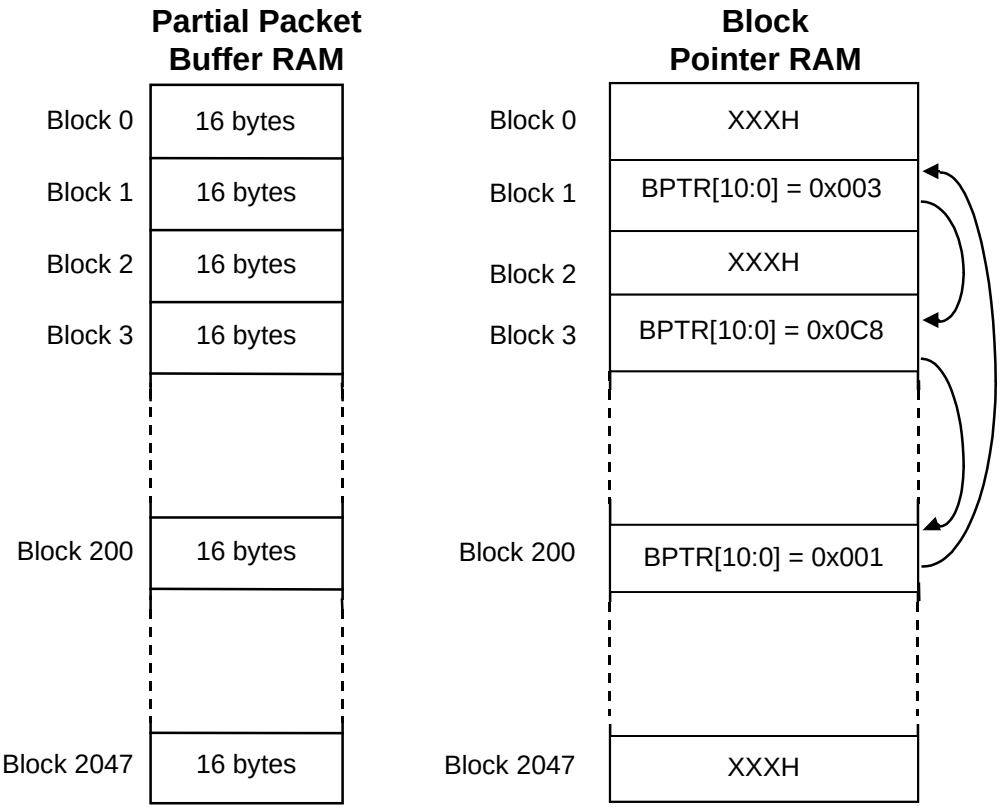
BIT8	Function
0	Channels configured for 7BIT will transmit a zero on the least significant bit of each octet.
1	Channels configured for 7BIT will transmit a one on the least significant bit of each octet.

11.3 Programming a Channel FIFO

A Channel FIFO is created from 3 or more blocks of internal RAM, and each block holds 16 bytes of packet data. There is a total of 2048 blocks (32 Kbytes) available to assign among the receive channels, and another 2048 blocks (32 Kbytes) available to assign among the transmit channels.

A FIFO is created by assigning a circular linked list of blocks as shown in Figure 14. This shows a channel FIFO consisting of 3 blocks. The quantity of buffers and the arrangement of links is chosen by the programmer, and the selection of blocks can be arbitrary. The programmer must ensure that a block is not assigned to more than one circularly linked list.

Figure 14 – Specifying a Channel FIFO



11.3.1 Receive Channel FIFO

A receive channel FIFO is programmed by repeating the following procedure for each block within the circularly linked list:

1. Poll the BUSY bit of the **RHDL Indirect Block Select** (0x210) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

2. Write the following register with the next block in the circular linked list, or exit if all links have been programmed:

Bit	Register	Value
BPTR[10:0]	**RHDL Indirect Block Data** (0x214)	0 through 0x7FF are valid
Reserved	**RHDL Indirect Block Data** (0x214)	0

3. Specify the block and update the internal block pointer RAM by writing the following register. Proceed to step 1.

Bit	Register	Value
BLOCK[10:0]	**RHDL Indirect Block Select** (0x210)	0 through 0x7FF are valid
Reserved	**RHDL Indirect Block Select** (0x210)	0
BRWB	**RHDL Indirect Block Select** (0x210)	0
BUSY	**RHDL Indirect Block Select** (0x210)	X

11.3.2 Transmit Channel FIFO

A transmit channel FIFO is programmed by repeating the following procedure for each block within the circularly linked list:

1. Poll the BUSY bit of the **THDL Indirect Block Select** (0x3A0) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

2. Write the following register with the next block in the circular linked list, or exit if all links have been programmed:

Bit	Register	Value
BPTR[10:0]	**THDL Indirect Block Data** (0x3A4)	0 through 0x7FF are valid

Bit	Register	Value
Reserved[0]	**THDL Indirect Block Data** (0x3A4)	0
Reserved[1]	**THDL Indirect Block Data** (0x3A4)	0

3. Specify the block and update the internal block pointer RAM by writing the following register. Proceed to step 1.

Bit	Register	Value
BLOCK[10:0]	**THDL Indirect Block Select** (0x3A0)	0 through 0x7FF are valid
Reserved	**THDL Indirect Block Select** (0x3A0)	0
BRWB	**THDL Indirect Block Select** (0x3A0)	0
BUSY	**THDL Indirect Block Select** (0x3A0)	X

11.4 RHDL672 Channel Configuration

The RHDL672 provides configurable options for each receive channel as identified in the following register fields:

Bit	Register
DELIN	**RHDL Indirect Channel Data Register #1** (0x204)
STRIP	**RHDL Indirect Channel Data Register #1** (0x204)
XFER[3:0]	**RHDL Indirect Channel Data Register #2** (0x208)
OFFSET[1:0]	**RHDL Indirect Channel Data Register #2** (0x208)
CRC[1:0]	**RHDL Indirect Channel Data Register #2** (0x208)
INVERT	**RHDL Indirect Channel Data Register #2** (0x208)
PRIORITY	**RHDL Indirect Channel Data Register #2** (0x208)
7BIT	**RHDL Indirect Channel Data Register #2** (0x208)

Note: When writing to **RHDL Indirect Channel Data Register #1** (0x204), the reserved bit (bit 11) must be set low for correct operation of the FREEDM-84P672.

Delineation

The data bits from the RCAS672 can be written directly to the Partial Packet Buffer or processed for flag sequence delineation, bit de-stuffing and CRC verification. The following bit enables or disables this feature:

DELIN	Function
0	Data is written to the Partial Packet Buffer without any HDLC processing (no flag sequence delineation, bit de-stuffing nor CRC verification) on the incoming stream.
1	Data is processed for flag sequence delineation, bit de-stuffing and optionally, CRC verification (CRC verification depends on CRC[1:0] value).

Strip FCS Bit

The indirect frame check sequence discard bit (STRIP) enables the RHDL672 to remove the FCS data before writing to the channel FIFO. STRIP is ignored when DELIN is low or when CRC[1:0] = 00B. This feature is configured as follows:

STRIP	Function
0	Includes FCS data with the data stream written to the channel FIFO.
1	Removes the FCS data from the data stream written to the channel FIFO.

DMA Transfer Size

The indirect channel transfer size configures the amount of data transferred in each transaction. When the channel FIFO depth reaches the depth specified by XFER[3:0] or when an end-of-packet exists in the FIFO, a request will be made to the RMAC672 to initiate a PCI write access to transfer the data to the PCI host. During the PCI bus DMA activity, other channels cannot gain access to the bus. Specifying a large transfer size may affect bus access latencies for other channels. The following bits specify the channel transfer size:

XFER[3:0]	Function
0 through 15 are valid	Specifies the data transfer size in blocks: Blocks = XFER[3:0] +1, and there are 16 bytes per block.

Notes:

- XFER[3:0] should be set such that the number of blocks transferred is at least two fewer than the total allocated to the associated channel.

- To ensure optimum PCI bus utilization efficiency, the programmer can choose an XFER size and receive buffer size such that the receive buffer size is an integral multiple of the XFER size. (i.e. - for a buffer size of *n* bytes and an XFER size of *x* bytes, the relationship, $n = i * x$, must be true where $i = 1, 2, 3, ...$). The programmer must choose a value of *n* that is a multiple of 16 for receive buffers, and must convert XFER value from blocks to bytes using the relationship of 16 bytes per block.

Insertion of Offset Bytes

The RHDL672 can be configured to insert offset bytes into the data stream before writing the data stream to the channel FIFO. The offset bytes are placed before each packet and their value is undefined. The following configuration options are available:

OFFSET[1:0]	Function
00	RHDL672 does not insert offset bytes
01	RHDL672 inserts 1 offset byte per packet
10	RHDL672 inserts 2 offset bytes per packet
11	RHDL672 inserts 3 offset bytes per packet

CRC Algorithm

The RHDL672 can perform CRC verification of the incoming data stream. The available options are as follows:

CRC[1:0]	DELIN	Function
X	0	No CRC verification
00	1	No CRC verification
01	1	CRC-CCITT verification
10	1	CRC-32 verification
11	1	Reserved

HDLC Data Inversion

The INVERT bit configures the RHDL672 to logically invert the incoming HDLC stream from the RCAS672 before processing it. The bit is specified as follows:

INVERT	Function
0	HDLC stream is not inverted.
1	HDLC stream is inverted.

Specifying Receive Channel Priority

All receive channels that must transfer data from their channel FIFO to packet memory contend for access to the PCI bus. The PRIORITY bit allows specified channels to have priority access to the PCI bus. The bit encoding is as follows:

PRIORITY	Function
0	This channel is serviced after channels with PRIORITY=1.
1	This channel is serviced before channels with PRIORITY=0.

Handling of Robbed bit Signaling

The 7BIT enable bit configures the RHDL672 to ignore the least significant bit of each octet (last bit of each octet received) in the incoming channel stream. This bit is encoded as follows:

7BIT	Function
0	The entire receive data stream is processed.
1	The least significant bit (last bit of each octet received) is ignored.

11.5 THDL672 Channel Configuration

The THDL672 provides configurable options for each transmit channel as identified in the following register fields:

Bit	Register
DELIN	**THDL Indirect Channel Data Register #1** (0x384)
CRC[1:0]	**THDL Indirect Channel Data Register #1** (0x384)
FLEN[10:0]	**THDL Indirect Channel Data Register #2** (0x388)

Bit	Register
DFCS	**THDL Indirect Channel Data Register #2** (0x388)
INVERT	**THDL Indirect Channel Data Register #2** (0x388)
PRIORITYB	**THDL Indirect Channel Data Register #2** (0x388)
7BIT	**THDL Indirect Channel Data Register #2** (0x388)
XFER[3:0]	**THDL Indirect Channel Data Register #3** (0x38C)
FLAG[2:0]	**THDL Indirect Channel Data Register #3** (0x38C)
LEVEL[3:0]	**THDL Indirect Channel Data Register #3** (0x38C)
IDLE	**THDL Indirect Channel Data Register #3** (0x38C)
TRANS	**THDL Indirect Channel Data Register #3** (0x38C)

Note: When writing to **THDL Indirect Channel Data Register #1** (0x384), the reserved bit (bit 11) must be set low for correct operation of the FREEDM-84P672. When writing to **THDL Indirect Channel Data Register #2** (0x388), the reserved bit (bit 11) must be set low for correct operation of the FREEDM-84P672.

Frame Delineation

The transmit packet data from packet memory can be written directly to the outgoing data stream or processed for flag sequence insertion, bit stuffing and CRC generation. The following bit enables or disables this feature:

DELIN	Function
0	Data is written directly to the outgoing data stream without any HDLC processing (no flag sequence insertion, bit stuffing nor CRC generation).
1	Data is processed for flag sequence insertion, bit stuffing and optionally, CRC generation (CRC generation depends on CRC[1:0] value).

CRC Algorithm

The THDL672 can perform CRC generation on the outgoing data stream. The available options are as follows:

CRC[1:0]	DELIN	Function
X	0	No CRC generation
00	1	No CRC generation
01	1	CRC-CCITT generation
10	1	CRC-32 generation
11	1	Reserved

Channel FIFO Length

The indirect FIFO length (FLEN[10:0]) is the number of blocks, less one, that is provisioned to the circular channel FIFO specified by the FPTR[10:0] block pointer.

FLEN[10:0]	Function
0 through 2047 are valid	Specifies the Channel FIFO size in blocks, where Blocks = FLEN[10:0] + 1, and each block is 16 bytes.

Inverting the FCS

The diagnose frame check sequence bit (DFCS) specifies whether the FCS field inserted into the transmit data stream is inverted. This is provided for diagnostic purposes and is programmed as follows:

DFCS	Function
0	FCS field in the outgoing HDLC stream is not inverted.
1	FCS field in the outgoing HDLC stream is logically inverted.

Specifying Transmit Channel Priority

All transmit buffer data must be read from packet memory, and across the PCI bus. Each transmit channel contends for access to the PCI bus and the PRIORITYB bit allows channels, where the Channel FIFO free space is greater than the starving trigger level and there are no complete packets within the FIFO, to have higher priority access to the PCI bus. The bit encoding is as follows:

PRIORITYB	Function
0	The channel has higher priority access when the Channel FIFO free space is greater than the starving trigger level, and the last byte of the packet has not been placed into the Channel FIFO.
1	The channel is inhibited from making expedited requests for data to the TMAC672. It has lower priority than channels with PRIORITYB=0 when the channel with PRIORITYB=0 has a partial packet in its Channel FIFO and the Channel FIFO is making an expedited data request.

Robbed Bit Signaling

The least significant stuff enable bit (7BIT) configures the THDL672 to stuff the least significant bit of each octet assigned to the transmit channel in the outgoing channel stream.

7BIT	Function
0	The entire octet contains valid data and BIT8 is ignored.
1	The least significant bit (last bit of each octet transmitted) does not contain channel data and is forced to the value configured by the BIT8 register bit.

DMA Transfer Size

The indirect channel transfer size specifies the amount of data that the partial packet processor requests from the TMAC672 block. When the channel FIFO free space reaches or exceeds the limit specified by XFER[3:0], the partial packet processor will make a request for data to the TMAC672 to retrieve the XFER[3:0] + 1 blocks of data. During the PCI bus DMA activity, other channels cannot gain access to the bus. Specifying a large transfer size may affect bus access latencies for other channels. The following bits specify the channel transfer size:

XFER[3:0]	Function
0 through 15 are valid	Specifies the data transfer size in blocks, where Blocks = XFER[3:0] + 1, and each block is 16 bytes.

Notes:

- To prevent lockup, the channel transfer size (XFER[3:0]) can be configured to be less than or equal to the start transmission level set by LEVEL[3:0] and TRANS. Alternatively, the channel transfer size can be set such that the total number of blocks in the logical channel FIFO minus the start transmission level is an integer multiple of the channel transfer size.

- To ensure optimum PCI bus utilization efficiency, the programmer can choose an XFER size and transmit buffer size such that the transmit buffer size is an integral multiple of the XFER size. (i.e. - for a buffer size of *n* bytes and an XFER size of *x* bytes, the relationship, $n = i * x$, must be true where $i = 1, 2, 3, \ldots$). The programmer must convert XFER value from blocks to bytes using the relationship of 16 bytes per block.

Specifying The Number of Flag or Idle Bytes Inserted Between Frames

The THDL672 can be configured to insert either flag or idle bytes (8 bits of one's) into the data stream between HDLC packets. The number of these is programmed as follows:

FLAG[2:0]	Minimum Number of Flag/Idle Bytes
000	1 flag / 0 Idle byte
001	2 flags / 0 idle byte
010	4 flags / 2 idle bytes
011	8 flags / 6 idle bytes
100	16 flags / 14 idle bytes
101	32 flags / 30 idle bytes
110	64 flags / 62 idle bytes
111	128 flags / 126 idle bytes

Interframe Time Fill

The IDLE bit specifies the byte pattern inserted in the data stream between HDLC packets.

IDLE	Function
0	Flag bytes are inserted between HDLC packets.

IDLE	Function
1	HDLC idle (all one's bit with no bit-stuffing) is inserted between HDLC packets.

Specifying the Channel FIFO's Starving Level and Start Transmit Level

The HDLC processor starts transmitting a packet when the channel FIFO free space is less than or equal to the level specified in the appropriate Start Transmission Level column of the following table or when an end of a packet is stored in the channel FIFO.

When the channel FIFO free space is less than or equal to than the level specified in the Starving Trigger Level column of the following table and the HDLC processor is transmitting a packet and an end of a packet is not stored in the channel FIFO, the partial packet buffer makes expedite requests to the TMAC672 to retrieve XFER[3:0] + 1 blocks of data.

The starving trigger level and start transmission level are programmed via the LEVEL[3:0] and the TRANS field as follows:

LEVEL[3:0]	Starving Trigger Level	Start Transmission Level (TRANS=0)	Start Transmission Level (TRANS=1)
0000	2 Blocks (32 bytes free)	1 Block (16 bytes free)	1 Block (16 bytes free)
0001	3 Blocks (48 bytes free)	2 Blocks (32 bytes free)	1 Block (16 bytes free)
0010	4 Blocks (64 bytes free)	3 Blocks (48 bytes free)	2 Blocks (32 bytes free)
0011	6 Blocks (96 bytes free)	4 Blocks (64 bytes free)	3 Blocks (48 bytes free)
0100	8 Blocks (128 bytes free)	6 Blocks (96 bytes free)	4 Blocks (64 bytes free)
0101	12 Blocks (192 bytes free)	8 Blocks (128 bytes free)	6 Blocks (96 bytes free)
0110	16 Blocks (256 bytes free)	12 Blocks (192 bytes free)	8 Blocks (128 bytes free)

LEVEL[3:0]	Starving Trigger Level	Start Transmission Level (TRANS=0)	Start Transmission Level (TRANS=1)
0111	24 Blocks (384 bytes free)	16 Blocks (256 bytes free)	12 Blocks (192 bytes free)
1000	32 Blocks (512 bytes free)	24 Blocks (384 bytes free)	16 Blocks (256 bytes free)
1001	48 Blocks (768 bytes free)	32 Blocks (512 bytes free)	24 Blocks (384 bytes free)
1010	64 Blocks (1 Kbytes free)	48 Blocks (768 bytes free)	32 Blocks (512 bytes free)
1011	96 Blocks (1.5 Kbytes free)	64 Blocks (1 Kbytes free)	48 Blocks (768 bytes free)
1100	192 Blocks (3 Kbytes free)	128 Blocks (2 Kbytes free)	96 Blocks (1.5 Kbytes free)
1101	384 Blocks (6 Kbytes free)	256 Blocks (4 Kbytes free)	192 Blocks (2 Kbytes free)
1110	768 Blocks (12 Kbytes free)	512 Blocks (8 Kbytes free)	384 Blocks (4 Kbytes free)
1111	1536 Blocks (24 Kbytes free)	1024 Blocks (16 Kbytes free)	768 Blocks (8 Kbytes free)

12 FREEDM-84P672 OPERATIONAL PROCEDURES

12.1 Device Identification, Location and System Resource Assignment

This section describes the software interaction required to identify a FREEDM-84P672 device on the PCI bus, map the Normal Mode Registers in packet memory, and initialize the PCI configuration registers.

Identifying and Locating a FREEDM-84P672

The software can identify each device attached to a PCI bus segment by reading the Device ID and the Vendor ID within the Configuration Space Header. As described in section 6.1 the software must activate the IDSEL pin of a PCI device in order to access the Configuration Space. The IDSEL pin of each PCI device is activated in turn and the first DWORD register is read to identify whether it has the FREEDM-84P672 Device ID (0x7384) and Vendor ID (0x11F8). If a value other than 0xFFFF is read in these fields then a PCI device is present at the IDSEL pin.

In addition to these fields the FREEDM-84P672 specifies a revision identifier within the REVID[7:0] field which may be useful to distinguish between future revisions of the FREEDM-84P672.

Memory Mapping the Register Space

During power-up the packet software needs to build a consistent address map and assign memory resources based on the requirements of each PCI device. The memory requirements are identified via the 6 base address registers in the PCI Configuration Space of each device.

The software writes a base address register with a value of all 1's and reads back the register. The software scans the returned value from the least significant bit upwards to determine the size of memory to assign to the base address register. The binary weighted value of the first one bit found (after the four least significant bits which are used for configuration) indicates the required amount of space. For example, a device that wants a 1M address space would build the top 12 bits and hardwire the others to zero.

For a FREEDM-84P672 device, only the first base address register – the **CBI Memory Base Address Register** (0x10) – is implemented, all other base address registers will be read as a value of all 1's. The first base address register will return the memory space requirement for the Normal Mode Registers – a memory size of 4Kbytes.

The packet software must assign a base address for this 4Kbyte memory space by writing the **CBI Memory Base Address Register** (0x10) within the PCI Configuration Space with the base address. The value can be read from this register at a later time to determine the mapping of the Normal Mode Register Space.

Enabling the FREEDM-84P672 onto the PCI Bus

Following assignment of the memory base address the software must enable the FREEDM-84P672 to respond to PCI memory accesses and to participate on the PCI bus as a bus master. Additionally, the FREEDM-84P672 can be enabled to report system and parity errors. The **Command** (0x04) register of the PCI Configuration Space is written as follows:

Bit	Word Sized Configuration Register	Value
MCNTRL	**Command** (0x04)	1
MSTREN	**Command** (0x04)	1
PERREN	**Command** (0x04)	1
SERREN	**Command** (0x04)	1

Initializing the PCI Configuration Space Registers

In addition to enabling the FREEDM-84P672 onto the PCI bus, the following register bits must also be initialized:

Bit	Byte Sized Configuration Register	Value
CLSIZE[7:0]	**Cache Line Size** (0x0C)	see note
LT[7:0]	**Latency Timer** (0x0D)	see note
INTLNE[7:0]	**Interrupt Line** (0x3C)	see note

Notes:

- CLSIZE[7:0] should be set equal to the cache line size of the embedded processor. The FREEDM-84P672 uses the memory read multiple command if the data transfer size is greater than the cache line size. It will use the memory read cache line if the data transfer is the same size, or less than the cache line, but greater than a dword. It uses a memory read if the data transfer size is a single dword.

- LT[7:0] should be set based on the expected initial latency of data transfers on the PCI bus, and on the expected maximum data transaction size

specified via the XFER field of the RMAC672 and TMAC672 blocks. The value is specified as a multiple of the PCI bus clock frequency. For a transfer size of 8 blocks and no initial latency, the value should be larger than *(8*4 + 3) = 35.*

- INTLNE[7:0] should be assigned for use by software after power-on. The value is determined based on which input of the system interrupt controller the FREEDM-84P672 interrupt pin is connected to.

12.2 Reset

This section describes the procedure to reset the FREEDM-84P672 via software. The FREEDM-84P672 is powered on in an inactive state and should be reset via software following a hardware reset, or as required by the embedded processor. The reset procedure is normally followed by the initialization procedure.

The steps to reset a FREEDM-84P672 are:

1. If the FREEDM-84P672 was active before the reset procedure then the deactivation procedure must be done (see section 12.5).

2. The RESET bit in the **FREEDM-84P672 Master Reset** (0x000) register must be written high and then written low.

This reset procedure has the following effects:

- The RESET bit allows the FREEDM-84P672 to be reset under software control. If the RESET bit is a logic one, the entire FREEDM-84P672 except the PCI Interface is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the FREEDM-84P672 out of reset. Holding the FREEDM-84P672 in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset.

- The GPIC672 PCI Configuration register values are preserved under software reset. All Normal Mode registers are set to their default values.

- None of the channel provisioning or the Channel FIFO configuration is preserved under software reset.

12.3 Initialization

This section describes the procedure to initialize the FREEDM-84P672. This procedure assumes the software has already allocated the data structures in

packet memory. A detailed discussion of allocation of data structures can be found in section 4.

The initialization procedure normally follows the software reset procedure and is followed by the activation procedure.

The steps to initialize a FREEDM-84P672 are:

1. Assign base addresses for the Transmit Descriptor Table, the Receive Packet Descriptor Table, the Transmit Queue Base, and the Receive Queue Base. The register accesses are described in sections 4.1 and 4.6.

2. Assign start, read, write, and end indexes for all queues. The register accesses are described in section 4.6.

3. Configure the SBI interface, and the SBI Extracter and Inserter for the SPEs conveyed on the SBI interface. The register accesses are described in sections 7 and 8.

4. Configure the RCAS672 and TCAS672 serial links. The register accesses are described in section 9.

5. Configure the GPIC672 interface. The register accesses are described in section 10.3.

6. Configure HDLC processing of the RHDL672 and the THDL672 blocks. The register accesses are described in sections 11.1 and 11.2.

12.4 Activation Procedure

The activation procedure is required to place the FREEDM-84P672 in a state after which the software may service FREEDM-84P672 interrupts, provision/unprovision channels, make transmit requests and monitor the status of the FREEDM-84P672.

The activation procedure normally follows the initialization procedure.

The steps to activate a FREEDM-84P672 are:

1. Enable interrupt 'E' bits, SBIEXTE and SBI_PERR_EN as described in section 5.

2. Enable the FREEDM-84P672 DMA activity by setting the ENABLE bits of the RMAC672 and TMAC672 as described in sections 10.1 and 10.2.

3. The SYSCLKA, REFCLKA, FASTCLKA and C1FPA bits in the **FREEDM-84P672 Master Clock/Frame Pulse Activity Monitor and Accumulation Trigger** (0x00C) register should be read periodically to detect for stuck at conditions. The SYSCLKA bit must be read high for proper operation of the FREEDM-84P672. A low value indicates a failure in clocking that is provided at the SYSCLK input pin of the FREEDM-84P672. Similarly, a low value in the other register bits indicates a failure in clocking that is provided by the corresponding input pin.

12.5 Deactivation Procedure

The deactivation procedure is required to place the FREEDM-84P672 in a state in which it will not interrupt the embedded processor, or make accesses to the packet memory. This procedure should occur after the FREEDM-84P672 actively transfers packets, or to gracefully shut down the FREEDM-84P672.

The steps to deactivate a FREEDM-84P672 are:

1. Disable interrupt 'E' bits, SBIEXTE and SBI_PERR_EN as described in section 5.

2. Disable the FREEDM-84P672 DMA activity by programming the ENABLE bits to zero in the RMAC672 and the TMAC672 as described in sections 10.1 and 10.2.

3. Continue by performing the software reset procedure.

12.6 Provisioning a Channel

The provisioning procedure normally follows the activation procedure and enables the FREEDM-84P672 to receive and/or transmit packets.

12.6.1 Receive Channel Provisioning

The steps to provision a receive channel *RCC*, where $0 \leq RCC \leq 671$ are:

1. Disable FREEDM-84P672 processing of the channel's data stream to allow for graceful provisioning. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**RCAS Channel Disable** (0x10C)	*RCC*
CHDIS	**RCAS Channel Disable** (0x10C)	1

2. Program the Channel FIFO as described in section 11.3.1.

3. Poll the BUSY bit of the **RHDL Indirect Channel Select** (0x200) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

4. Specify the HDLC configuration for this channel by writing appropriate bits in the **RHDL Indirect Channel Data Register #1** (0x204) and the **RHDL Indirect Channel Data Register #2** (0x208) as described in section 11.4. When writing the **RHDL Indirect Channel Data Register #1** (0x204), ensure that the PROV bit is set, and ensure that the FPTR[10:0] bits identify a block within the circular linked list of buffers of step 2.

5. Specify the RHDL672 channel to provision by writing the following register. Then poll the BUSY bit to ensure that it is low before proceeding to step 6.

Bit	Register	Value
CHAN[9:0]	**RHDL Indirect Channel Select** (0x200)	*RCC*
CRWB	**RHDL Indirect Channel Select** (0x200)	0
BUSY	**RHDL Indirect Channel Select** (0x200)	X

6. Poll the BUSY bit of the **RCAS Indirect Link and Time-slot Select** (0x100) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

7. Specify the RCAS672 channel that is provisioned. Write the following register:

Bit	Register	Value
CHAN[9:0]	**RCAS Indirect Channel Data** (0x104)	*RCC*
PROV	**RCAS Indirect Channel Data** (0x104)	1
CDLBEN	**RCAS Indirect Channel Data** (0x104)	0

8. For a **channelised** link, specify the time-slots which are assigned for processing on this channel by writing the following register once for each time-slot that is assigned to the channel. Valid values for TSLOT[4:0] are 1 through 24 for a T1/J1 link, and 1 through 31 for an E1 link. For an **unchannelised** or **unframed** link, TSLOT[4:0] must only have the value 0, and this register is written just once. Each write must be followed by a read to determine whether the BUSY bit (bit15) is low, and to ensure that the indirect RAM has been updated.

Bit	Register	Value
TSLOT[4:0]	**RCAS Indirect Link and Time-slot Select** (0x100)	see above
LINK[6:0]	**RCAS Indirect Link and Time-slot Select** (0x100)	0 through 83 are valid
RWB	**RCAS Indirect Link and Time-slot Select** (0x100)	0
BUSY	**RCAS Indirect Link and Time-slot Select** (0x100)	X

9. Enable FREEDM-84P672 processing of the channel data stream to allow for graceful provisioning. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**RCAS Channel Disable** (0x10C)	*RCC*
CHDIS	**RCAS Channel Disable** (0x10C)	0

Warning:

- The RCAS Channel Disable bit (CHDIS) is only applicable to one channel at a time. In other words, the receive channel provisioning procedure needs to be run once for each channel.

- The programmer must ensure that the channel has not been provisioned, or has been unprovisioned before doing the provisioning procedure. The reset procedure has the effect of unprovisioning all channels of the FREEDM-84P672.

- Continuous polling of a register in a tight loop involves multiple PCI memory read transactions and may have an adverse effect on the PCI bus bandwidth available for other activities. The recommended method of polling the BUSY bit is to read the register on expiration of a system timer, or after a number of CPU clock ticks. Recommended time intervals are in the range 1 msec through 100 msec.

- A Channel is not provisioned until the BUSY bit toggles low.

12.6.2 Transmit Channel Provisioning

The steps to provision a transmit channel *TCC*, where $0 \leq TCC \leq 671$ are:

1. Disable FREEDM-84P672 processing of the channel's data stream to allow for graceful provisioning. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**TCAS Channel Disable** (0x410)	*TCC*
CHDIS	**TCAS Channel Disable** (0x410)	1

2. Program the Channel FIFO as described in section 11.3.2 for a transmit channel.

3. Poll the BUSY bit of the **THDL Indirect Channel Select** (0x380) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

4. Specify the HDLC configuration for this transmit channel by writing the **THDL Indirect Channel Data Register #1** (0x384), **THDL Indirect Channel Data Register #2** (0x388) and the **THDL Indirect Channel Data Register #3** (0x38C) as described in section 11.5. In writing the **THDL Indirect Channel Data Register #1** (0x384), ensure the PROV bit is set, and ensure the FPTR[10:0] bits identify a block within the circular linked list of buffers of step 2.

5. Specify the THDL672 channel that is provisioned by writing the following register. Then poll the BUSY bit to ensure it is low before proceeding with step 6.

Bit	Register	Value
CHAN[9:0]	**THDL Indirect Channel Select** (0x380)	*TCC*
CRWB	**THDL Indirect Channel Select** (0x380)	0
BUSY	**THDL Indirect Channel Select** (0x380)	X

6. Poll the BUSY bit of the **TCAS Indirect Link and Time-slot Select** (0x400) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

7. Specify the TCAS672 channel that is provisioned. Write the following register:

Bit	Register	Value
CHAN[9:0]	**TCAS Indirect Channel Data** (0x404)	*TCC*
PROV	**TCAS Indirect Channel Data** (0x404)	1

8. For a **channelised** link, specify the time-slots which are assigned for processing on this channel by writing the following register once for each time-slot that is assigned to the channel. Valid values for TSLOT[4:0] are 1 through 24 for a T1/J1 link, and 1 through 31 for an E1 link. For an **unchannelised** or **unframed** link, TSLOT[4:0] must only have the value 0, and this register is written just once. Each write must be followed by a read to determine whether the BUSY bit (bit15) is low, and to ensure that the indirect RAM has been updated.

Bit	Register	Value
TSLOT[4:0]	**TCAS Indirect Link and Time-slot Select** (0x400)	see above
LINK[6:0]	**TCAS Indirect Link and Time-slot Select** (0x400)	0 through 83 are valid
RWB	**TCAS Indirect Link and Time-slot Select** (0x400)	0
BUSY	**TCAS Indirect Link and Time-slot Select** (0x400)	X

9. Poll the BUSY bit of the **TMAC Indirect Channel Provisioning** (0x304) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

10. Specify the TMAC672 channel to provision. Write the following register fields, then poll the BUSY bit to ensure the provisioning process has completed.

Bit	Register	Value
CHAN[9:0]	**TMAC Indirect Channel Provisioning** (0x304)	*TCC*
PROV	**TMAC Indirect Channel Provisioning** (0x304)	1
RWB	**TMAC Indirect Channel Provisioning** (0x304)	0
BUSY	**TMAC Indirect Channel Provisioning** (0x304)	X

11. Enable FREEDM-84P672 processing of the channel data stream to allow for graceful provisioning. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**TCAS Channel Disable** (0x410)	*TCC*
CHDIS	**TCAS Channel Disable** (0x410)	0

Warning:

- The TCAS Channel Disable bit (CHDIS) is only applicable to one channel at a time. In other words, the transmit channel provisioning procedure needs to be run once for each channel.
- The programmer must ensure that the channel has not been provisioned, or has been unprovisioned before doing the provisioning procedure. The reset procedure has the affect of unprovisioning all channels of the FREEDM-84P672.
- Continuous polling of a register in a tight loop involves multiple PCI memory read transactions and may have an adverse effect on the PCI bus bandwidth available for other activities. The recommended method of polling the BUSY bit is to read the register on expiration of a system timer, or after a number of CPU clock ticks. Recommended time intervals are in the range 1 msec through 100 msec.
- A Channel is not provisioned until the BUSY bit toggles low.

12.7 Unprovisioning a Channel

The unprovisioning procedure is normally applied to channels that are provisioned.

12.7.1 Receive Channel Unprovisioning

The steps to unprovision a receive channel *RCC*, where $0 \leq RCC \leq 671$ are:

1. Disable FREEDM-84P672 processing of the channel's data stream to allow for graceful unprovisioning. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**RCAS Channel Disable** (0x10C)	*RCC*
CHDIS	**RCAS Channel Disable** (0x10C)	1

2. Poll the BUSY bit of the **RCAS Indirect Link and Time-slot Select** (0x100) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

3. Specify the RCAS672 channel to unprovision by writing the following register:

Bit	Register	Value
CHAN[9:0]	**RCAS Indirect Channel Data** (0x104)	*RCC*
PROV	**RCAS Indirect Channel Data** (0x104)	0
CDLBEN	**RCAS Indirect Channel Data** (0x104)	X

4. For a **channelised** link, specify the time-slots which are unassigned on this channel by writing the following register once for each time-slot that is unassigned. Valid values for TSLOT[4:0] are 1 through 24 for a T1/J1 link, and 1 through 31 for an E1 link. For an **unchannelised** or **unframed** link, TSLOT[4:0] must only have the value 0, and this register is written just once. Each write must be followed by a read to determine whether the BUSY bit (bit15) is low, and to ensure that the indirect RAM has been updated.

Bit	Register	Value
TSLOT[4:0]	**RCAS Indirect Link and Time-slot Select** (0x100)	see above
LINK[6:0]	**RCAS Indirect Link and Time-slot Select** (0x100)	0 through 83 are valid
RWB	**RCAS Indirect Link and Time-slot Select** (0x100)	0
BUSY	**RCAS Indirect Link and Time-slot Select** (0x100)	X

5. Poll the BUSY bit of the **RHDL Indirect Channel Select** (0x200) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

6. Read the RHDL672 channel data by writing the following register. Then poll the BUSY bit to ensure it is low before proceeding with step 7.

Bit	Register	Value
CHAN[9:0]	**RHDL Indirect Channel Select** (0x200)	*RCC*
CRWB	**RHDL Indirect Channel Select** (0x200)	1

Bit	Register	Value
BUSY	**RHDL Indirect Channel Select** (0x200)	X

7. Read the RHDL672 indirect channel data and check that the TAVAIL bit of the **RHDL Indirect Channel Data #1** (0x204) register is zero. This ensures that the last DMA transfer request for this channel has completed. If the TAVAIL bit is zero, proceed to step 8, otherwise, return to step 6.

8. Write the **RHDL Indirect Channel Data #1** (0x204) register with PROV modified to zero, while keeping the same FPTR[10:0] bits.

9. Specify the RHDL672 channel to unprovision by writing the following register. Then poll the BUSY bit to ensure that it is low before proceeding with step 10.

Bit	Register	Value
CHAN[9:0]	**RHDL Indirect Channel Select** (0x200)	*RCC*
CRWB	**RHDL Indirect Channel Select** (0x200)	0
BUSY	**RHDL Indirect Channel Select** (0x200)	X

10. Poll the BUSY bit of the **RMAC Indirect Channel Provisioning** (0x284) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started. Please see the notes below for the case where the BUSY bit is stuck at one due to empty receive free queues.

11. Ensure that partially filled buffer(s) for the channel are returned to the RPDR Ready queue by writing the following register. Then poll the BUSY bit to ensure that it is low before proceeding with step 12.

Bit	Register	Value
CHAN[9:0]	**RMAC Indirect Channel Provisioning** (0x284)	*RCC*
PROV	**RMAC Indirect Channel Provisioning** (0x284)	0
RWB	**RMAC Indirect Channel Provisioning** (0x284)	0
BUSY	**RMAC Indirect Channel Provisioning** (0x284)	X

12. Enable FREEDM-84P672 processing of the unprovisioned channel. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**RCAS Channel Disable** (0x10C)	*RCC*
CHDIS	**RCAS Channel Disable** (0x10C)	0

Note: If the out-of-buffer situation occurs (RPDFQEI error occurs and the BUSY bit of the **RMAC Indirect Channel Provisioning** (0x284) register is stuck at one) unexpectedly because an extremely large erroneous packet of a channel consumes all of the free buffers, the following steps can be used to free up the buffers:

1. Disable the RMAC672 by setting the ENABLE bit of the **RMAC Control** (0x280) register to zero.

2. Place a descriptor pointing to the emergency buffer onto either the RPDR Free Small queue or RPDR Free Large queue. Then, wait a short time for the buffer to be consumed and written to, and for the RMAC672 to return to its state machine's main loop.

3. Unprovision channels using the standard procedure in this section, with the following changes:

   - Keep the RMAC672 disabled by setting the ENABLE bit of the **RMAC Control** (0x280) register to zero, while unprovisioning the channels.

   - Do not wait for the TAVAIL bit in the **RHDL Indirect Channel Data #1** (0x204) register to clear.

   - As part of this process, channels will be flushed in the **RMAC Indirect Channel Provisioning** (0x284) register. This will cause a linked list of buffers to be returned on the RPDR Ready queue. Traverse the linked list to reclaim the buffers.

4. When sufficient buffers have been recovered, re-enable the RMAC672 by setting the ENABLE bit of the **RMAC Control** (0x280) register to one. Remember to set one buffer aside for future emergency use.

Warning:

- The RCAS Channel Disable bit (CHDIS) is only applicable to one channel at a time. In other words, the receive channel unprovisioning procedure needs to be run once for each channel.

- Continuous polling of a register in a tight loop involves multiple PCI memory read transactions and may have an adverse effect on the PCI bus bandwidth available for other activities. The recommended method of polling the BUSY bit is to read the register on expiration of a system timer, or after a number of CPU clock ticks. Recommended time intervals are in the range 1 msec through 100 msec.

- A Channel is not unprovisioned until the BUSY bit toggles low.

12.7.2 Transmit Channel Unprovisioning

The steps to unprovision a transmit channel *TCC*, where $0 \leq TCC \leq 671$ are:

1. Unprovision the TMAC672 channel. Poll the BUSY bit of the **TMAC Indirect Channel Provisioning** (0x304) register until it is zero. Then write the following bits:

Bit	Register	Value
CHAN[9:0]	**TMAC Indirect Channel Provisioning** (0x304)	*TCC*
PROV	**TMAC Indirect Channel Provisioning** (0x304)	0
RWB	**TMAC Indirect Channel Provisioning** (0x304)	0
BUSY	**TMAC Indirect Channel Provisioning** (0x304)	X

2. Poll the BUSY bit of the **TMAC Indirect Channel Provisioning** (0x304) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

3. Disable FREEDM-84P672 processing of the channel's data stream to allow for graceful unprovisioning. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**TCAS Channel Disable** (0x410)	*TCC*
CHDIS	**TCAS Channel Disable** (0x410)	1

4. Poll the BUSY bit of the **TCAS Indirect Link and Time-slot Select** (0x400) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

5. Specify the TCAS672 channel to be unprovisioned. Write the following register:

Bit	Register	Value
CHAN[9:0]	**TCAS Indirect Channel Data** (0x404)	*TCC*
PROV	**TCAS Indirect Channel Data** (0x404)	0

6. For a **channelised** link, specify the time-slots which are unassigned for processing on this channel by writing the following register once for each time-slot that is unassigned. Valid values for TSLOT[4:0] are 1 through 24 for a T1/J1 link, and 1 through 31 for an E1 link. For an **unchannelised** or **unframed** link, TSLOT[4:0] must only have the value 0, and this register is written just once. Each write must be followed by a read to determine whether the BUSY bit (bit15) is low, and to ensure that the indirect RAM has been updated.

Bit	Register	Value
TSLOT[4:0]	**TCAS Indirect Link and Time-slot Select** (0x400)	see above
LINK[6:0]	**TCAS Indirect Link and Time-slot Select** (0x400)	0 through 83 are valid
RWB	**TCAS Indirect Link and Time-slot Select** (0x400)	0
BUSY	**TCAS Indirect Link and Time-slot Select** (0x400)	X

7. Poll the BUSY bit of the **THDL Indirect Channel Select** (0x380) register until it is zero. This ensures that a previous indirect RAM access has completed and that a new indirect RAM access can be started.

8. Read the THDL672 channel data by writing the following register. Then poll the BUSY bit to ensure that it is low before proceeding with step 9.

Bit	Register	Value
CHAN[9:0]	**THDL Indirect Channel Select** (0x380)	*TCC*
CRWB	**THDL Indirect Channel Select** (0x380)	1
BUSY	**THDL Indirect Channel Select** (0x380)	X

9. Read the **THDL Indirect Channel Data #1** (0x384) register. Then write this register with PROV modified to zero, while keeping the same FPTR[10:0] bits.

10. Specify the THDL672 channel to unprovision by writing the following register. Then poll the BUSY bit to ensure that it is low before proceeding with step 11.

Bit	Register	Value
CHAN[9:0]	**THDL Indirect Channel Select** (0x380)	*TCC*
CRWB	**THDL Indirect Channel Select** (0x380)	0
BUSY	**THDL Indirect Channel Select** (0x380)	X

11. Enable FREEDM-84P672 processing of the channel. Write the following bits:

Bit	Register	Value
DCHAN[9:0]	**TCAS Channel Disable** (0x410)	*TCC*
CHDIS	**TCAS Channel Disable** (0x410)	0

Warning:

- The TCAS Channel Disable bit (CHDIS) is only applicable to one channel at a time. In other words, the transmit channel unprovisioning procedure needs to be run once for each channel.

- Continuous polling of a register in a tight loop involves multiple PCI memory read transactions and may have an adverse effect on the PCI bus bandwidth available for other activities. The recommended method of polling the BUSY bit is to read the register on expiration of a system timer, or after a number of CPU clock ticks. Recommended time intervals are in the range 1 msec through 100 msec.

- A Channel is not unprovisioned until the BUSY bit toggles low.

12.8 Receive Sequence

The following sequence of activities takes place when a packet is received on a provisioned receive channel:

1. The FREEDM-84P672 reads a RPDR associated with a free buffer as follows:

    - If this is the first buffer of the receive packet it will read a RPDR associated with a small free buffer from the Small Buffer Cache, or if the cache is empty, from the RPDRF Small queue. RPDRs are read from the queue up to six at a time and stored in the cache.

- If this is not the first buffer of the receive packet it will read a RPDR associated with a large free buffer from the Large Buffer Cache, or if the cache is empty, from the RPDRF Large queue. RPDRs are read from the queue up to six at a time and stored in the cache.

2. The FREEDM-84P672 generates an interrupt if the programmed number of RPDRs have been read from the RPDR Small (or Large) queue. The RPQSFI or the RPQLFI status bits of the **FREEDM-84P672 Master Interrupt Status** (0x008) register indicate which queue must be replenished with free RPDRs by the software. The software can use the WriteQueue() routine of section 4.6 to replenish the queue. The frequency of the interrupt, and the number of RPDRs to replenish per interrupt, can be programmed via the RPQ_LFN[1:0] and the RPQ_SFN[1:0] bits of the **RMAC Control** (0x280) register.

3. If the receive packet requires multiple buffers to be filled, and the RPDR is not the first for this packet, then the following fields of the previous RPD are written by the FREEDM-84P672: RCC[9:0], CE, Status[5:0], Bytes in Buffer[15:0], and Next RPD Pointer[14:0].

4. The FREEDM-84P672 reads the RPD associated with the free RPDR to determine the buffer address, size and offset.

5. The FREEDM-84P672 writes receive data to the buffer. The priority and configuration of the channel determines when the PCI bus access may occur, and the number of blocks transferred in each access.

6. The above sequence is repeated until the end of packet occurs.

7. When the end of packet occurs the following fields of the RPD are written by the FREEDM-84P672: RCC[9:0], CE, Status[5:0], Bytes in Buffer[15:0], and Next RPD Pointer[14:0].

8. The STATUS[1:0] field of the RPDR is assigned and the first RPDR in the linked list of RPDs which describe the receive packet data is written to the RPDR Ready queue by the FREEDM-84P672.

9. The embedded processor is interrupted if the programmed number of RPDRs have been written to the RPDR Ready queue. The RPQRDYI interrupt status bit is set within the **FREEDM-84P672 Master Interrupt Status** (0x008) register. The number of RPDRs required to generate an interrupt is specified by the RPQ_RDYN[2:0] field of the **RMAC Control** (0x280) register.

10. The software responds to the interrupt by reading from the RPDR Ready queue as per the ReadQueue() procedure of section 4.6. Each RPDR

represents one packet, whereby the RPDR points to the first RPD in the packet. When the Status[1:0] bits of the RPDR read from the queue has an error status of 01B the software must go to the last RPDR that links the individual RPDs and examine the Status[5:0] field of the last RPD to determine the cause of error.

Note: During the receive channel unprovisioning procedure, all RPDRs read from the RPDRF Large or Small queue that are partially processed for the unprovisioned channel are written to RPDR Ready queue. The software must examine the STATUS[1:0] bits of the RPDR to determine whether it is an unprovisioned partial packet. If the RPDR is an unprovisioned partial packet then the software must unlink the chain based on the CE bit and the RMAC Next RPD Pointer[14:0] of each RPD in the chain. This will ensure that all RPDs and data buffers are returned to the RPDR Ready queue.

12.9 Transmit Sequence

The following sequence of activities takes place when a packet is transmitted on a provisioned transmit channel:

1. The software initializes and links one or more TDs to identify the transmit packet(s). The software must not re-use a TD within the Transmit Descriptor Table until it has been freed onto the TDR Free queue.

2. The software writes one or more TDRs to the TDR Ready queue as per the WriteQueue() routine of section 4.6. Each TDR that is written to the TDR Ready queue points to the first TD in chain of TDs which describe the packet(s).

3. The software writes the **TMAC Transmit Descriptor Reference Ready Queue Write** (0x32C) register during the WriteQueue() routine. In response to a change in this register the FREEDM-84P672 reads packet memory at the TDR Ready queue locations that were written by the software.

4. The TMAC672 links the first TDR of each packet read from the TDR Ready queue to a linked list maintained by the TMAC672. The TMAC672 linked list is maintained on a channel basis. The TMAC672 writes the TMAC Next TD Pointer[14:0] field and the V bit field within the first TD of the last packet in the TMAC672 linked list. There is no linking if the TMAC672 linked list is empty.

5. The TMAC672 reads and transmits buffer data according to the Host linked list and the TMAC672 linked list. The priority and configuration of each provisioned channel determines when the buffer data is read.

6. After reading the contents of a buffer the TMAC672 assigns the STATUS[2:0] bits of the TDR and then writes the TDR as follows:

   - the TDR is written directly to the TDR Free queue if the CACHE bit is zero within the **TMAC Control** (0x300) register. Or,

   - if the IOC bit is set within the TD then all TDRs within the TDR Cache are flushed to the TDR Free queue the TDR is written to the TDR Free queue. Or,

   - the TDR is written to the TDR cache because the CACHE bit is set within the **TMAC Control** (0x300) register. Freed TDRs are cached and written up to six at a time to the TDR Free queue.

7. The embedded processor is interrupted if either of the following has occurred:

   - one or more TDR are written to the TDR Free queue because the IOC bit was set in the last TD processed by the TMAC672. The IOCI status bit is set within the **FREEDM-84P672 Master Interrupt Status** (0x008) register.

   - one or more TDR are written to the TDR Free queue because the CACHE bit is set, and the TDQ_FRN[1:0] bits of the TMAC Control (0x300) register specify that an interrupt should occur. The TDQFI status bit is set within the **FREEDM-84P672 Master Interrupt Status** (0x008) register.

   - one TDR is written to the TDR Free queue because the CACHE bit is zero in the **TMAC Control** (0x300) register. The TDQFI status bit is set within the **FREEDM-84P672 Master Interrupt Status** (0x008) register.

8. The software responds to the interrupt by reading from the TDR Free queue as per the ReadQueue() procedure of section 4.6. The FREEDM-84P672 returns TDRs to the free queue (or the TDR cache) one at a time, as the data buffer is processed. Therefore the software must examine the Status[2:0] field of the TDR to determine whether the TDR is associated with the last data buffer in the linked list - indicating the transmit packet has been completely processed - or to determine whether any errors occurred in processing the individual data buffers of the linked TDs that form the packet.

Note: During the transmit channel unprovisioning procedure, a TDR that is being processed by the FREEDM-84P672 and that belongs to the unprovisioned channel is written to TDR Free queue. The software must examine the STATUS[2:0] bits to determine whether the TDR is associated with an unprovisioned partial packet. If the TDR is an unprovisioned partial packet, then the software must unlink the chain based on the V bit and the TMAC Next TD Pointer[14:0] of each TD in the chain. It must also unlink descriptors in the host

chain, based on the CE bit and the Host Next TD Pointer[14:0], of the unprovisioned TDR. This will ensure that all TDs (and data buffers) of the unprovisioned channel are returned to the host.

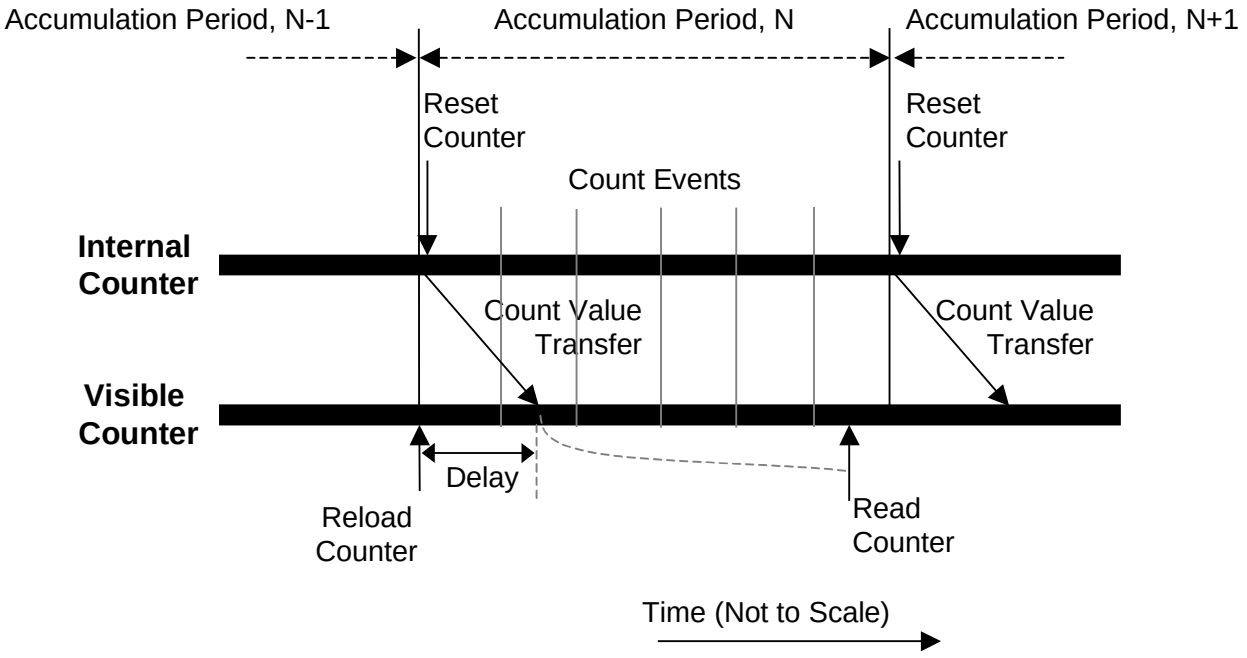
12.10 Performance Counters

The FREEDM-84P672 provides four count registers within the Normal Mode Register Space. These are as follows:

Bit	Register
OF[15:0]	**PMON Receive FIFO Overflow Count** (0x504)
UF[15:0]	**PMON Transmit FIFO Underflow Count** (0x508)
C1[15:0]	**PMON Configurable Count #1** (0x50C)
C2[15:0]	**PMON Configurable Count #2** (0x510)

The software must poll these counters to prevent overflow. Figure 15 illustrates the sequence of events when the counters are polled. The **PMON Status** (0x500) register provides status bits which indicate whether any of the four internal holding counters has overflowed.

Figure 15 – Event Sequence for Polling of Counters



The software initiates a counter reload by writing to the **FREEDM-84P672 Master Clock/Frame Pulse Activity Monitor and Accumulation Trigger** (0x00C) register. There is a small delay to transfer data from internal counters to the visible counters. The recommended polling strategy is to read the counters first before initiating a reload. Using this strategy, the transfer latency can be ignored.

Counters are normally configured during initialization. The first configurable count register is assigned by setting one of the following register bits, while setting all other bits to zero:

Bit	Register
RSPE1EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
RFCSE1EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
RABRT1EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
RLENE1EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
RP1EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
TABRT1EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
TP1EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)

The second configurable count register is assigned by setting one of the following register bits, while setting all other bits to zero:

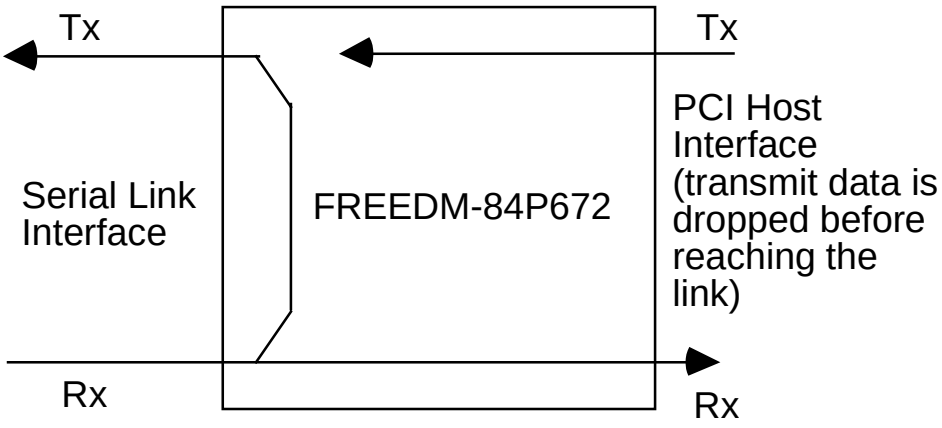
Bit	Register
RSPE2EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
RFCSE2EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
RABRT2EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
RLENE2EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)

Bit	Register
RP2EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
TABRT2EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)
TP2EN	**FREEDM-84P672 Master Performance Monitor Control** (0x024)

12.11 Line Loopback

Serial links of the RCAS672/TCAS672 can be placed in line loopback. In this configuration, the data on the receive link output by the SBI PISO blocks is looped back to the transmit link input of the SBI SIPO blocks as illustrated in Figure 16.

Figure 16 – Line Loopback



Serial links can be placed in line loopback by setting the appropriate bit within one of the following registers. There are 84 bits corresponding to the 84 serial links.

Bit	Register
LLBEN[15:0]	**FREEDM-84P672 Master Line Loopback #1** (0x030)
LLBEN[31:16]	**FREEDM-84P672 Master Line Loopback #2** (0x034)
LLBEN[47:32]	**FREEDM-84P672 Master Line Loopback #3** (0x038)
LLBEN[63:48]	**FREEDM-84P672 Master Line Loopback #4** (0x03C)

Bit	Register
LLBEN[79:64]	**FREEDM-84P672 Master Line Loopback #5** (0x040)
LLBEN[83:80]	**FREEDM-84P672 Master Line Loopback #6** (0x044)

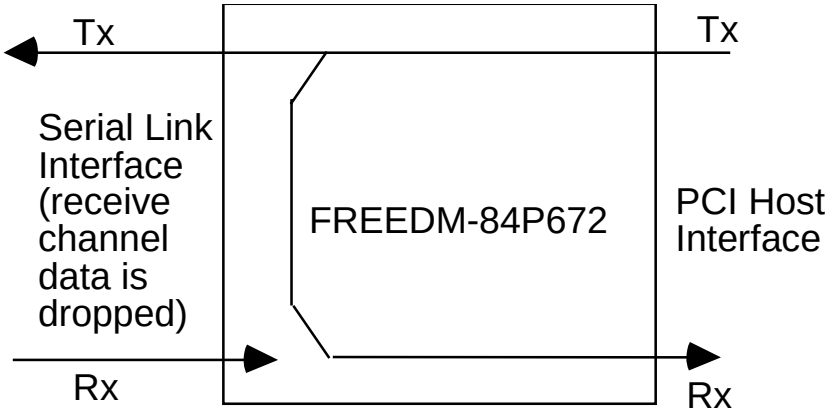
Note: The software should unprovision channels associated with the link that is placed in line loopback mode before placing the link in line loopback. This will prevent the data stream at the serial link from passing through the FREEDM-84P672 to the PCI interface.

12.12 Diagnostic Loopback

Each channel of the FREEDM-84P672 can be placed in a diagnostic loopback mode. In this configuration, the transmit data stream is looped back to the receive data stream as illustrated in Figure 17. The pair of transmit/receive channels is configured in diagnostic loopback mode by provisioning both the transmit and the receive channels as specified in section 12.6, except with the CDLBEN bit set high within the **RCAS Indirect Channel Data** (0x104) register.

In diagnostic loopback mode, the transmit channel data is looped back as well as driven onto the transmit serial link. The channel data from the receive serial link is dropped. The bit timing for the diagnostic loopback mode is generated internally. This clock is derived from REFCLK, C1FP and FASTCLK (if the SPE is configured to support DS-3 links) so these inputs should be active.

Figure 17 – Diagnostic Loopback

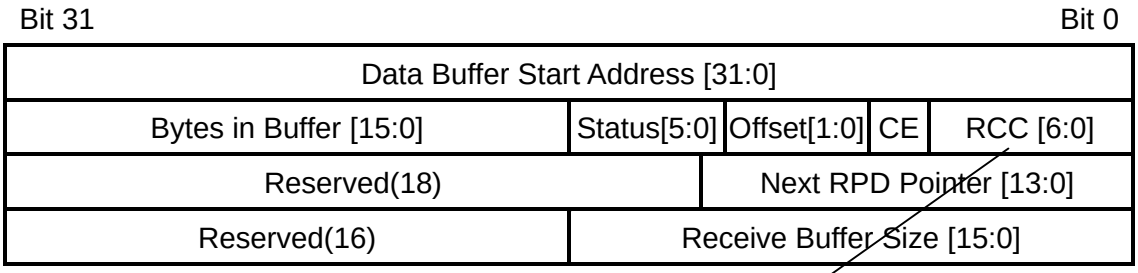


APPENDIX A – RECEIVE PACKET DESCRIPTOR CHANGES

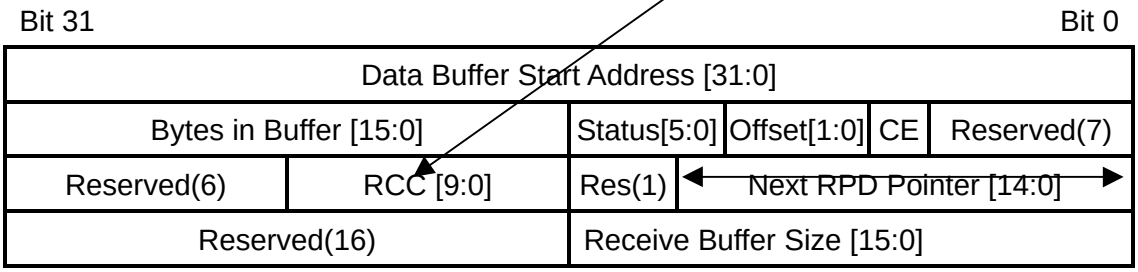
Figure 18 illustrates the changes made to the Receive Packet Descriptor (RPD) from the FREEDM-32 to the FREEDM-84P672.

Figure 18 – Changes to Receive Packet Descriptor

FREEDM-32



FREEDM-84P672



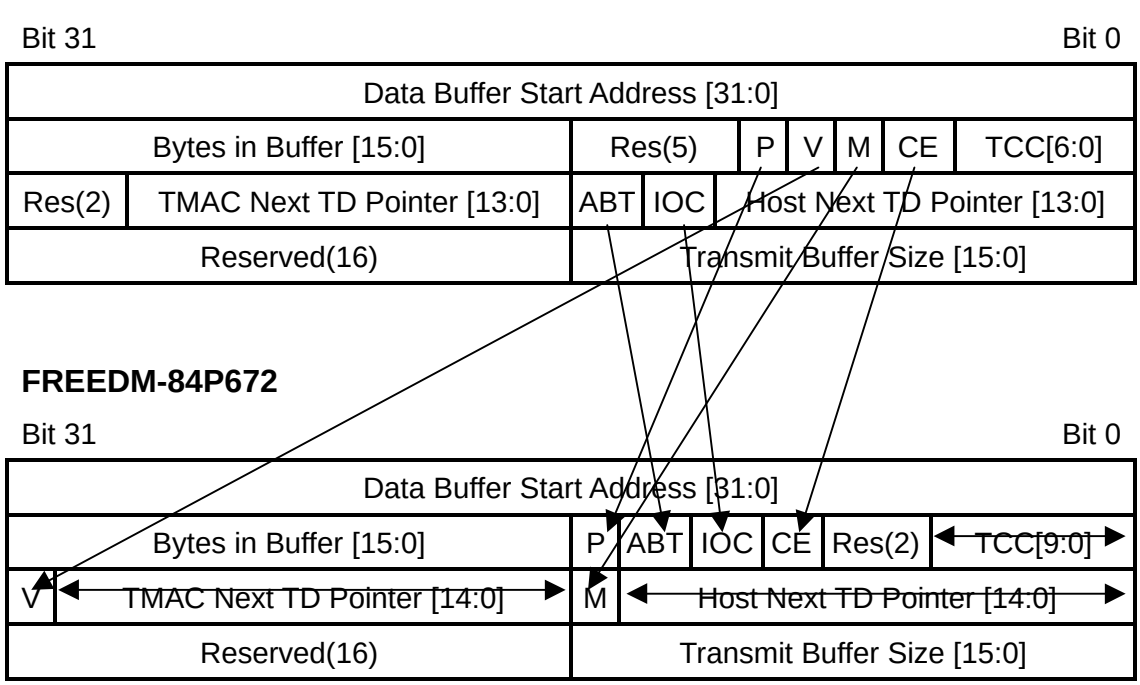
The Receive Channel Code (RCC) field increased from 7 bits to 10 bits as a result of the increase in addressable HDLC channels from 128 to 672 for the FREEDM-84P672. This field has also been relocated.

The Next RPD Pointer field increased from 14 bits to 15 bits as a result of the increase in maximum number of addressable descriptors from 16K to 32K for the FREEDM-84P672.

APPENDIX B – TRANSMIT DESCRIPTOR CHANGES

Figure 19 illustrates the changes made to the Transmit Descriptor (TD) from the FREEDM-32 to the FREEDM-84P672.

Figure 19 – Changes to Transmit Descriptor



The Transmit Channel Code (TCC) field increased from 7 bits to 10 bits as a result of the increase in addressable HDLC channels from 128 to 672 for the FREEDM-84P672.

The TMAC Next TD Pointer and Host Next TD Pointer fields increased from 14 bits to 15 bits as a result of the increase in maximum number of addressable descriptors from 16K to 32K for the FREEDM-84P672.

The following control bits have been relocated: P, V, M, CE, ABT and IOC. Please see section 4.3 for a description of these fields.

APPENDIX C – REGISTER LEVEL CHANGES

The following table is a comparison of the normal mode registers at the register level among the FREEDM-32, the FREEDM-32P672 and the FREEDM-84P672. Registers in bold indicate differences at the register level among the members of the FREEDM family listed in the table. Table entries that are "N/A" indicate that the register is not applicable in the corresponding FREEDM device. Please see Appendix G for differences at the bit level for the normal mode registers.

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
FREEDM-x Master Reset	0x000	0x000	0x000
FREEDM-x Master Interrupt Enable	0x004	0x004	0x004
FREEDM-x Master Interrupt Status	0x008	0x008	0x008
FREEDM-x Master Clock/Frame Pulse/BERT Activity Monitor and Accumulation Trigger	0x00C	0x00C	0x00C
FREEDM-x Master Link Activity Monitor	**0x010**	**0x010**	**N/A**
FREEDM-x Master Line Loopback #1	**0x014**	**0x014**	**0x030**
FREEDM-x Master Line Loopback #2	**0x018**	**0x018**	**0x034**
Reserved	**0x01C**	**N/A**	**0x010 – 0x020**
FREEDM-x Reserved	**N/A**	**0x01C**	**N/A**
FREEDM-x Master BERT Control	**0x020**	**0x020**	**N/A**
FREEDM-x Master Performance Monitor Control	0x024	0x024	0x024
FREEDM-x Master SBI Interrupt Enable	**N/A**	**N/A**	**0x028**

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
FREEDM-x Master SBI Interrupt Status	**N/A**	**N/A**	**0x02C**
FREEDM-x Master Line Loopback #3	**N/A**	**N/A**	**0x038**
FREEDM-x Master Line Loopback #4	**N/A**	**N/A**	**0x03C**
FREEDM-x Master Line Loopback #5	**N/A**	**N/A**	**0x040**
FREEDM-x Master Line Loopback #6	**N/A**	**N/A**	**0x044**
FREEDM-x SBI DROP BUS Master Configuration	**N/A**	**N/A**	**0x048**
FREEDM-x SBI ADD BUS Master Configuration	**N/A**	**N/A**	**0x04C**
Reserved	**0x028 – 0x03C**	**0x028 – 0x07C**	**0x050 – 0x07C**
GPIC Control	**0x040**	**0x080**	**0x080**
GPIC Reserved	**0x044 – 0x07C**	**0x084 – 0x0FC**	**0x084 – 0x0FC**
Reserved	**0x080 – 0x0FC**	**N/A**	**N/A**
RCAS Indirect Channel and Time-slot Select	0x100	0x100	0x100
RCAS Indirect Channel Data	0x104	0x104	0x104
RCAS Framing Bit Threshold	**0x108**	**0x108**	**N/A**
RCAS Reserved	**N/A**	**N/A**	**0x108**
RCAS Channel Disable	0x10C	0x10C	0x10C
RCAS Reserved	**0x110 – 0x17C**	**0x110 – 0x17C**	**0x110 – 0x13C**

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
RCAS SBI SPE1 Configuration Register #1	**N/A**	**N/A**	**0x140**
RCAS SBI SPE1 Configuration Register #2	**N/A**	**N/A**	**0x144**
RCAS SBI SPE2 Configuration Register #1	**N/A**	**N/A**	**0x148**
RCAS SBI SPE2 Configuration Register #2	**N/A**	**N/A**	**0x14C**
RCAS SBI SPE3 Configuration Register #1	**N/A**	**N/A**	**0x150**
RCAS SBI SPE3 Configuration Register #2	**N/A**	**N/A**	**0x154**
RCAS Reserved	**N/A**	**N/A**	**0x158 – 0x17C**
RCAS Links #0 through #2 Configuration	0x180 – 0x188	0x180 – 0x188	0x180 – 0x188
RCAS Links #3 through #31 Configuration	**0x18C – 0x1FC**	**0x18C – 0x1FC**	**N/A**
RCAS Reserved	**N/A**	**N/A**	**0x18C – 0x1FC**
RHDL Indirect Channel Select	0x200	0x200	0x200
RHDL Indirect Channel Data Register #1	0x204	0x204	0x204
RHDL Indirect Channel Data Register #2	0x208	0x208	0x208
RHDL Reserved	0x20C	0x20C	0x20C
RHDL Indirect Block Select	0x210	0x210	0x210
RHDL Indirect Block Data Register	0x214	0x214	0x214
RHDL Reserved	0x218 – 0x21C	0x218 – 0x21C	0x218 – 0x21C
RHDL Configuration	0x220	0x220	0x220

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
RHDL Maximum Packet Length	0x224	0x224	0x224
RHDL Reserved	0x228 – 0x23C	0x228 – 0x23C	0x228 – 0x23C
Reserved	0x240 – 0x27C	0x240 – 0x27C	0x240 – 0x27C
RMAC Control	0x280	0x280	0x280
RMAC Indirect Channel Provisioning	0x284	0x284	0x284
RMAC Packet Descriptor Table Base LSW	0x288	0x288	0x288
RMAC Packet Descriptor Table Base MSW	0x28C	0x28C	0x28C
RMAC Queue Base LSW	0x290	0x290	0x290
RMAC Queue Base MSW	0x294	0x294	0x294
RMAC Packet Descriptor Reference Large Buffer Free Queue Start	0x298	0x298	0x298
RMAC Packet Descriptor Reference Large Buffer Free Queue Write	0x29C	0x29C	0x29C
RMAC Packet Descriptor Reference Large Buffer Free Queue Read	0x2A0	0x2A0	0x2A0
RMAC Packet Descriptor Reference Large Buffer Free Queue End	0x2A4	0x2A4	0x2A4
RMAC Packet Descriptor Reference Small Buffer Free Queue Start	0x2A8	0x2A8	0x2A8
RMAC Packet Descriptor Reference Small Buffer Free Queue Write	0x2AC	0x2AC	0x2AC

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
RMAC Packet Descriptor Reference Small Buffer Free Queue Read	0x2B0	0x2B0	0x2B0
RMAC Packet Descriptor Reference Small Buffer Free Queue End	0x2B4	0x2B4	0x2B4
RMAC Packet Descriptor Reference Ready Queue Start	0x2B8	0x2B8	0x2B8
RMAC Packet Descriptor Reference Ready Queue Write	0x2BC	0x2BC	0x2BC
RMAC Packet Descriptor Reference Ready Queue Read	0x2C0	0x2C0	0x2C0
RMAC Packet Descriptor Reference Ready Queue End	0x2C4	0x2C4	0x2C4
RMAC Reserved	0x2C8 – 0x2FC	0x2C8 – 0x2FC	0x2C8 – 0x2FC
TMAC Control	0x300	0x300	0x300
TMAC Indirect Channel Provisioning	0x304	0x304	0x304
TMAC Descriptor Table Base LSW	0x308	0x308	0x308
TMAC Descriptor Table Base MSW	0x30C	0x30C	0x30C
TMAC Queue Base LSW	0x310	0x310	0x310
TMAC Queue Base MSW	0x314	0x314	0x314
TMAC Descriptor Reference Free Queue Start	0x318	0x318	0x318
TMAC Descriptor Reference Free Queue Write	0x31C	0x31C	0x31C

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
TMAC Descriptor Reference Free Queue Read	0x320	0x320	0x320
TMAC Descriptor Reference Free Queue End	0x324	0x324	0x324
TMAC Descriptor Reference Ready Queue Start	0x328	0x328	0x328
TMAC Descriptor Reference Ready Queue Write	0x32C	0x32C	0x32C
TMAC Descriptor Reference Ready Queue Read	0x330	0x330	0x330
TMAC Descriptor Reference Ready Queue End	0x334	0x334	0x334
TMAC Reserved	0x338 – 0x37C	0x338 – 0x37C	0x338 – 0x37C
THDL Indirect Channel Select	0x380	0x380	0x380
THDL Indirect Channel Data #1	0x384	0x384	0x384
THDL Indirect Channel Data #2	0x388	0x388	0x388
THDL Indirect Channel Data #3	0x38C	0x38C	0x38C
THDL Reserved	0x390 – 0x39C	0x390 – 0x39C	0x390 – 0x39C
THDL Indirect Block Select	0x3A0	0x3A0	0x3A0
THDL Indirect Block Data	0x3A4	0x3A4	0x3A4
THDL Reserved	0x3A8 – 0x3AC	0x3A8 – 0x3AC	0x3A8 – 0x3AC
THDL Configuration	0x3B0	0x3B0	0x3B0
THDL Reserved	0x3B4 – 0x3BC	0x3B4 – 0x3BC	0x3B4 – 0x3BC

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
Reserved	0x3C0 – 0x3FC	0x3C0 – 0x3FC	0x3C0 – 0x3FC
TCAS Indirect Channel and Time-slot Select	0x400	0x400	0x400
TCAS Indirect Channel Data	0x404	0x404	0x404
TCAS Framing Bit Threshold	**0x408**	**0x408**	**N/A**
TCAS Reserved	**N/A**	**N/A**	**0x408**
TCAS Idle Time-slot Fill Data	0x40C	0x40C	0x40C
TCAS Channel Disable	0x410	0x410	0x410
TCAS Reserved	**0x414 – 0x47C**	**0x414 – 0x47C**	**0x414 – 0x43C**
TCAS SBI SPE1 Configuration Register #1	**N/A**	**N/A**	**0x440**
TCAS SBI SPE1 Configuration Register #2	**N/A**	**N/A**	**0x444**
TCAS SBI SPE2 Configuration Register #1	**N/A**	**N/A**	**0x448**
TCAS SBI SPE2 Configuration Register #2	**N/A**	**N/A**	**0x44C**
TCAS SBI SPE3 Configuration Register #1	**N/A**	**N/A**	**0x450**
TCAS SBI SPE3 Configuration Register #2	**N/A**	**N/A**	**0x454**
TCAS Reserved	**N/A**	**N/A**	**0x458 – 0x47C**
TCAS Links #0 through #2 Configuration	0x480 – 0x488	0x480 – 0x488	0x480 – 0x488
TCAS Links #3 through #31 Configuration	**0x48C – 0x4FC**	**0x48C – 0x4FC**	**N/A**
TCAS Reserved	**N/A**	**N/A**	**0x48C – 0x4FC**
PMON Status	0x500	0x500	0x500

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
PMON Receive FIFO Overflow Count	0x504	0x504	0x504
PMON Transmit FIFO Underflow Count	0x508	0x508	0x508
PMON Configurable Count #1	0x50C	0x50C	0x50C
PMON Configurable Count #2	0x510	0x510	0x510
PMON Reserved	0x514 – 0x51C	0x514 – 0x51C	0x514 – 0x51C
Reserved	**0x520 – 0x7FC**	**0x520 – 0x7FC**	**0x520 – 0x5BC**
SBI EXTRACT Control	**N/A**	**N/A**	**0x5C0**
SBI EXTRACT Reserved	**N/A**	**N/A**	**0x5C4 - 0x5C8**
SBI EXTRACT Tributary RAM Indirect Access Address	**N/A**	**N/A**	**0x5CC**
SBI EXTRACT Tributary RAM Indirect Access Control	**N/A**	**N/A**	**0x5D0**
SBI EXTRACT Reserved	**N/A**	**N/A**	**0x5D4**
SBI EXTRACT Tributary RAM Indirect Access Data	**N/A**	**N/A**	**0x5D8**
SBI EXTRACT Parity Error Interrupt Reason	**N/A**	**N/A**	**0x5DC**
SBI EXTRACT Reserved	**N/A**	**N/A**	**0x5E0 – 0x5FC**
Reserved	**N/A**	**N/A**	**0x600 – 0x67C**
SBI INSERT Control	**N/A**	**N/A**	**0X680**
SBI INSERT Reserved	**N/A**	**N/A**	**0x684 – 0x688**
SBI INSERT Tributary RAM Indirect Access Address	**N/A**	**N/A**	**0x68C**

Register	FREEDM-32 PCI Offset	FREEDM-32P672 PCI Offset	FREEDM-84P672 PCI Offset
SBI INSERT Tributary RAM Indirect Access Control	**N/A**	**N/A**	**0x690**
SBI INSERT Reserved	**N/A**	**N/A**	**0x694**
SBI INSERT Tributary RAM Indirect Access Data	**N/A**	**N/A**	**0x698**
SBI INSERT Reserved	**N/A**	**N/A**	**0x69C – 0x6FC**
Reserved	**N/A**	**N/A**	**0x700 – 0x7FC**

Note: The PCI Configuration registers have not changed at the register level among the FREEDM-32, FREEDM-32P672 and the FREEDM-84P672. Please see Appendix H for differences at the bit level for the PCI Configuration registers.

APPENDIX D – NEW NORMAL MODE REGISTERS

The following registers are new for the FREEDM-84P672. The new registers are used to configure and control the SBI interface, the SBI Extracter and Inserter, and to control line loopback for the increased number of links. Please refer to the Longform Datasheet[1] for detailed descriptions of these registers.

FREEDM-84P672 PCI Offset	Register
0x028	FREEDM-84P672 Master SBI Interrupt Enable
0x02C	FREEDM-84P672 Master SBI Interrupt Status
0x038	FREEDM-84P672 Master Line Loopback #3
0x03C	FREEDM-84P672 Master Line Loopback #4
0x040	FREEDM-84P672 Master Line Loopback #5
0x044	FREEDM-84P672 Master Line Loopback #6
0x048	FREEDM-84P672 SBI DROP BUS Master Configuration
0x04C	FREEDM-84P672 SBI ADD BUS Master Configuration
0x140	RCAS SBI SPE1 Configuration Register #1
0x144	RCAS SBI SPE1 Configuration Register #2
0x148	RCAS SBI SPE2 Configuration Register #1
0x14C	RCAS SBI SPE2 Configuration Register #2
0x150	RCAS SBI SPE3 Configuration Register #1
0x154	RCAS SBI SPE3 Configuration Register #2
0x440	TCAS SBI SPE1 Configuration Register #1
0x444	TCAS SBI SPE1 Configuration Register #2
0x448	TCAS SBI SPE2 Configuration Register #1
0x44C	TCAS SBI SPE2 Configuration Register #2
0x450	TCAS SBI SPE3 Configuration Register #1
0x454	TCAS SBI SPE3 Configuration Register #2
0x5C0	SBI EXTRACT Control

FREEDM-84P672 PCI Offset	Register
0x5C4 - 0x5C8	SBI EXTRACT Reserved
0x5CC	SBI EXTRACT Tributary RAM Indirect Access Address
0x5D0	SBI EXTRACT Tributary RAM Indirect Access Control
0x5D4	SBI EXTRACT Reserved
0x5D8	SBI EXTRACT Tributary RAM Indirect Access Data
0x5DC	SBI EXTRACT Parity Error Interrupt Reason
0x5E0 - 0x5FC	SBI EXTRACT Reserved
0x680	SBI INSERT Control
0x684 - 0x688	SBI INSERT Reserved
0x68C	SBI INSERT Tributary RAM Indirect Access Address
0x690	SBI INSERT Tributary RAM Indirect Access Control
0x694	SBI INSERT Reserved
0x698	SBI INSERT Tributary RAM Indirect Access Data
0x69C - 0x6FC	SBI INSERT Reserved

APPENDIX E – NON-APPLICABLE NORMAL MODE REGISTERS

The following FREEDM-32 registers are no longer applicable in the FREEDM-84P672.

FREEDM-32 PCI Offset	Register
0x010	FREEDM-32 Master Link Activity Monitor
0x020	FREEDM-32 Master BERT Control
0x108	RCAS Framing Bit Threshold
0x18C – 0x1FC	RCAS Links #3 through #31 Configuration
0x408	TCAS Framing Bit Threshold
0x48C – 0x4FC	TCAS Links #3 through #31 Configuration

APPENDIX F – MOVED NORMAL MODE REGISTERS

The following registers have been moved when comparing its FREEDM-32 location to its FREEDM-84P672 location.

Register	FREEDM-32 PCI Offset	FREEDM-84P672 PCI Offset
FREEDM-x Master Line Loopback #1	0x014	0x030
FREEDM-x Master Line Loopback #2	0x018	0x034
GPIC Control	0x040	0x080
GPIC Reserved	0x044 – 0x07C	0x084 – 0x0FC
RCAS Reserved	0x110 – 0x17C	0x108 0x110-0x13C 0x158 – 0x17C 0x18C – 0x1FC
TCAS Reserved	0x414 – 0x47C	0x408 0x414 – 0x43C 0x458 – 0x47C 0x48C – 0x4FC

APPENDIX G – NORMAL MODE REGISTER BIT CHANGES

The following normal mode registers have changed at the bit level from the FREEDM-32 to the FREEDM-84P672. Unless specified, register names, locations and comments refer to FREEDM-84P672 registers.

Register 0x00C : FREEDM-84P672 Master Clock / Frame Pulse Activity Monitor and Accumulation Trigger

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
3	C1FPA	X	Unused	X	SBI frame pulse active bit.
2	FASTCLKA	X	Unused	X	SBI fast clock active bit.
1	REFCLKA	X	TBDA	X	SBI reference clock active bit. Transmit BERT data active bit is not applicable in the FREEDM-84P672.

Register 0x080 : GPIC Control

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
13	RPWTH[5]	0	Unused	X	Increase in range of sizes for Receive Packet Write Threshold.

Register 0x100 : RCAS Indirect Link and Time-slot Select

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
12	LINK[6]	0	LINK[4]	0	Increase in the number of receive links from 32 to 84.
11	LINK[5]	0	LINK[3]	0	
10	LINK[4]	0	LINK[2]	0	
9	LINK[3]	0	LINK[1]	0	
8	LINK[2]	0	LINK[0]	0	
7	LINK[1]	0	Unused	X	
6	LINK[0]	0	Unused	X	

Register 0x104 : RCAS Indirect Channel Data

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
15	CDLBEN	0	Unused	X	
14	PROV	0	Unused	X	
9	CHAN[9]	0	CDLBEN	0	Increase in size of CHAN from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	CHAN[8]	0	PROV	0	
7	CHAN[7]	0	Unused	X	

Register 0x10C : RCAS Channel Disable

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
9	DCHAN[9]	0	Unused	X	Increase in size of DCHAN from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	DCHAN[8]	0	Unused	X	
7	DCHAN[7]	0	Unused	X	

Registers 0x180 – 0x188 : RCAS Links #0 to #2 Configuration

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
4	Reserved	0	Unused	X	The reserved bits must be set low for correct operation of the FREEDM-84P672.
2	Reserved	0	BSYNC	0	
1	Reserved	0	E1	0	
0	Reserved	0	CEN	0	CEN, E1 and BSYNC are not applicable in the FREEDM-84P672.

Register 0x200 : RHDL Indirect Channel Select

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
9	CHAN[9]	0	Unused	X	Increase in size of CHAN from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	CHAN[8]	0	Unused	X	
7	CHAN[7]	0	Unused	X	

Register 0x204 : RHDL Indirect Channel Data #1

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
14	STRIP	0	CRC[1]	0	CRC[1] moved to bit 11 of Register 0x208 of the FREEDM-84P672.
13	DELIN	0	CRC[0]	0	CRC[0] moved to bit 10 of Register 0x208 of the FREEDM-84P672.
12	TAVAIL	X	STRIP	0	
11	Reserved	X	DELIN	0	Reserved bit must be set low for correct operation of the FREEDM-84P672.
10	FPTR[10]	X	TAVAIL	X	Increase in size of FPTR from 9 bits to 11 bits as the result of increase in addressable descriptors from 512 to 2048.
9	FPTR[9]	X	Unused	X	

Register 0x208 : RHDL Indirect Channel Data #2

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
11	CRC[1]	0	Unused	X	CRC[1] moved from bit 14 of Register 0x204 of the FREEDM-32.
10	CRC[0]	0	Unused	X	CRC[0] moved from bit 13 of Register 0x204 of the FREEDM-32.
3	XFER[3]	0	Unused	X	XFER increased from 3 bits to 4 bits to support larger data transfers.

Register 0x210 : RHDL Indirect Block Select

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
11	Reserved	X	Unused	X	Reserved bit must be set low for correct operation of FREEDM-84P672.
10	BLOCK[10]	X	Unused	X	BLOCK increased from 9 bits to 11 bits as the result of increase in addressable blocks from 512 to 2048.
9	BLOCK[9]	X	Unused	X	

Register 0x214 : RHDL Indirect Block Data

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
11	Reserved	X	Unused	X	Reserved bit must be set low for correct operation of FREEDM-84P672.
10	BPTR[10]	X	Unused	X	BPTR increased from 9 bits to 11 bits as the result of increase in addressable blocks from 512 to 2048.
9	BPTR[9]	X	Unused	X	

Register 0x220 : RHDL Configuration

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
2	Unused	X	Reserved[2]	1	These reserved bits are no longer used in the FREEDM-84P672.
1	Unused	X	Reserved[1]	1	
0	Unused	X	Reserved[0]	1	

Register 0x280 : RMAC Control

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
12	Reserved	0	Unused	X	Reserved bit must be set low for correct operation of FREEDM-84P672.

Register 0x284 : RMAC Indirect Channel Provisioning

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
13	PROV	1	Unused	X	
9	CHAN[9]	0	Unused	X	CHAN increased from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	CHAN[8]	0	Unused	X	
7	CHAN[7]	0	PROV	1	

Register 0x300 : TMAC Control

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
7	FQFLUSH	0	Unused	X	New feature. Can force a flush of the TD Free queue with FQFLUSH bit.

Register 0x304 : TMAC Indirect Channel Provisioning

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
13	PROV	0	Unused	X	
9	CHAN[9]	0	Unused	X	CHAN increased from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	CHAN[8]	0	Unused	X	
7	CHAN[7]	0	PROV	0	

Register 0x380 : THDL Indirect Channel Select

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
9	CHAN[9]	0	Unused	X	Increase in size of CHAN from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	CHAN[8]	0	Unused	X	
7	CHAN[7]	0	Unused	X	

Register 0x384 : THDL Indirect Channel Data #1

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
12	DELIN	X	IDLE	0	IDLE moved to bit 14 of Register 0x38C of the FREEDM-84P672.
11	Reserved	X	DELIN	0	Reserved bit must be set low for correct operation of FREEDM-84P672.
10	FPTR[10]	0	Unused	X	Increase in size of FPTR from 9 bits to 11 bits as the result of increase in addressable descriptors from 512 to 2048.
9	FPTR[9]	0	Unused	X	

Register 0x388 : THDL Indirect Channel Data #2

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
11	Reserved	0	Unused	X	Reserved bit must be set low for correct operation of FREEDM-84P672.
10	FLEN[10]	0	Unused	X	Increase in size of FLEN from 9 bits to 11 bits as the result of increase in addressable descriptors from 512 to 2048.
9	FLEN[9]	0	Unused	X	

Register 0x38C : THDL Indirect Channel Data #3

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
14	IDLE	0	Unused	X	IDLE moved from bit 12 of Register 0x384 of the FREEDM-32.
3	XFER[3]	0	Unused	X	XFER increased from 3 bits to 4 bits to support larger data transfers.

Register 0x3A0 : THDL Indirect Block Select

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
11	Reserved	X	Unused	X	Reserved bit must be set low for correct operation of FREEDM-84P672.
10	BLOCK[10]	0	Unused	X	BLOCK increased from 9 bits to 11 bits as the result of increase in addressable blocks from 512 to 2048.
9	BLOCK[9]	0	Unused	X	

Register 0x3A4 : THDL Indirect Block Data

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
11	Reserved	X	Unused	X	Reserved bit must be set low for correct operation of FREEDM-84P672.
10	BPTR[10]	0	Unused	X	BPTR increased from 9 bits to 11 bits as the result of increase in addressable blocks from 512 to 2048.
9	BPTR[9]	0	Unused	X	

Register 0x3B0 : THDL Configuration

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
3	BURST[3]	0	Unused	X	BURST increased from 3 bits to 4 bits to increase maximum amount of data requested.

Register 0x400 : TCAS Indirect Link and Time-slot Select

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
12	LINK[6]	0	LINK[4]	0	Increase in the number of transmit links from 32 to 84.
11	LINK[5]	0	LINK[3]	0	
10	LINK[4]	0	LINK[2]	0	
9	LINK[3]	0	LINK[1]	0	
8	LINK[2]	0	LINK[0]	0	
7	LINK[1]	0	Unused	X	
6	LINK[0]	0	Unused	X	

Register 0x404 : TCAS Indirect Channel Data

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
15	PROV	0	Unused	X	
9	CHAN[9]	0	Unused	X	Increase in size of CHAN from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	CHAN[8]	0	PROV	0	
7	CHAN[7]	0	Unused	X	

Register 0x408 : TCAS Framing Bit Threshold

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
6	FTHRES[6]	0	FTHRES[6]	0	
5	FTHRES[5]	1	FTHRES[5]	0	Change of default value.
4	FTHRES[4]	0	FTHRES[4]	1	Change of default value.
3	FTHRES[3]	0	FTHRES[3]	1	Change of default value.
2	FTHRES[2]	1	FTHRES[2]	1	
1	FTHRES[1]	0	FTHRES[1]	1	Change of default value.
0	FTHRES[0]	1	FTHRES[0]	1	

Register 0x410 : TCAS Channel Disable

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
9	DCHAN[9]	0	Unused	X	Increase in size of DCHAN from 7 bits to 10 bits as the result of increase in HDLC channels from 128 to 672.
8	DCHAN[8]	0	Unused	X	
7	DCHAN[7]	0	Unused	X	

Registers 0x480 – 0x488 : TCAS Links #0 to #2 Configuration

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
4	Reserved	0	Unused	X	The reserved bits must be set low for correct operation of the FREEDM-84P672.
2	Reserved	0	BSYNC	0	
1	Reserved	0	E1	0	
0	Reserved	0	CEN	0	CEN, E1 and BSYNC are not applicable in the FREEDM-84P672.

APPENDIX H – PCI CONFIGURATION REGISTER BIT CHANGES

The following PCI Configuration registers have changed at the bit level from the FREEDM-32 to the FREEDM-84P672. Unless specified, register names, locations and comments refer to FREEDM-84P672 registers.

Register 0x00 : Vendor Identification/Device Identification

Bits	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
31:16	DEVID[15:0]	7384H	DEVID[15:0]	7364H	New device identification for FREEDM-84P672.

Register 0x04: Command/Status

Bit	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
21	66MHZ_CAPABLE	1	Reserved	0	Hardware wired to one to indicate that GPIC672 is 66 MHz capable.

Register 0x08 : Revision Identifier/Class Code

Bits	FREEDM-84P672		FREEDM-32		Comments
	Function	Default	Function	Default	
7:0	REVID[7:0]	00H	REVID[7:0]	01H	Different revision identification.

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